UNIVERSITAT POLITÈCNICA DE CATALUNYA

Design of Low-Dropout Regulator for Ultra Low Power On-Chip Applications

MASTER THESIS

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Abstract

Low Drop Out (LDO) voltage regulators are commonly used to supply low-voltage digital circuits such as microprocessor cores. These digital circuits normally are continuously changing from one mode of operation to another. Therefore, the load demand can change rapidly resulting in large voltage transients at the output of the regulator which can adversely affect the digital circuitry.

In this Master's Thesis, design topologies and challenges of very low-power fully integrated On-Chip Low-Dropout (LDO) regulators have been analyzed. Instead of conventional LDO which makes use of a large external capacitor to have better dynamic response and stability, a CapacitorLess LDO (CL-LDO) is chosen on considerations of smaller area.

The most challenging part of designing this kind of regulator is achieving high current efficiency by reducing the quiescent current while ensuring good stability response as well as good regulation performance. Thus, different circuit techniques must be carefully added in order to balance the lack of the large external capacitor having the minimum impact on system efficiency.

This work focuses on designing a fully integrated low-dropout regulator with good dynamic performance, high regulation performance and ultra-low power consumption. The stability is achieved by the use of two pole-splitting techniques, namely Cascode and Nested-Miller compensation. The good dynamic response with low quiescent current are achieved by the use of an adaptive biasing circuit, a gm-boost circuit and adaptive power transistor architecture.

KEY WORDS- *Low-Dropout, regulator, CL-LDO, capless, Gm-Boost, ultra-low quiescent LDO.*

Acknowledgements

Before starting the introduction I would like to thank all those who contributed in some way to the realization of this thesis work.

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Chapter 1

Introduction

There are two trends that have marked the semiconductor industry and the consumer electronics in the last years: The reduction of the area of the projects and the reduction of the power consumption. These two requirements call for silicon integrated electronic systems with increasingly lower consumption and maximum integration allowing to remove external components on chips (System-on-Chip paradigm, or SoC). To achieve this, it is necessary to generate internally different optimized voltage domains for the different integrated functions with a level of performance and consumption required. Thus, it is becoming more necessary to study in detail what power converters and voltage converters are required to integrate into the chip (on-chip) and which to leave outside the chip (off-chip). It is also indispensable to evaluate for each voltage sub-domain what type of circuit is required: Linear circuits (linear regulators, linear regulators LDO, with output device pMOS or nMOS, etc.) or switched circuits (switching capacitor, switching inductor).

Likewise, it is necessary to design a regulation with specific feedback network based on the output voltage specifications as well as a frequency compensation method to guarantee its stability.

1.1 Linear Regulator and Switching Regulator

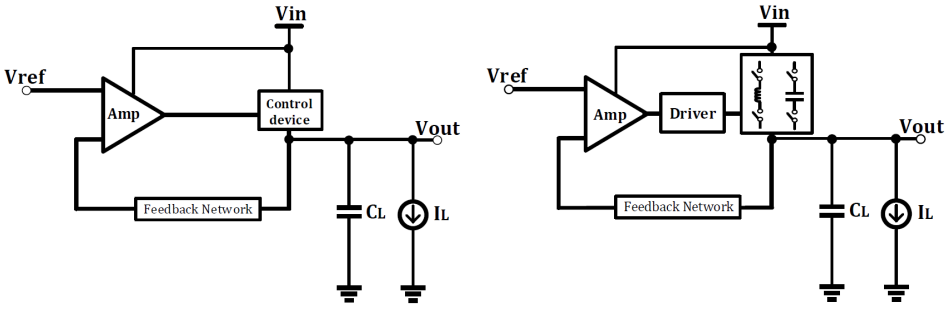
The linear regulator is a DC-DC voltage converter which linearly regulates the input DC voltage to a lower output DC voltage (Fig.1.1a). As the output voltage is linearly regulated, it has advantages in aspects of power supply rejection, output noise and dynamic response, etc. The main drawbacks are low efficiency and restriction to down conversion.

The power efficiency of linear regulators is greatly affected by changes in the DC input voltage, since it is inversely proportional to the voltage drop across the control device. The larger the difference between the input and the output, the less efficient the regulator. Furthermore, the power loss increases as a function of the current load. Therefore, for high current load, linear regulator may not be the suitable candidate for some systems.

$$P_{dissipation} = (Vin - Vout)Iload \tag{1.1}$$

Usually, if the input voltage is much larger than the regulated output, a switching regulator is placed before the linear regulator to improve the overall efficiency. Switching regulators have the ability to boost (step-up) or buck (step-down) the input voltage to any output voltage as well as they are capable of operating at efficiencies of over 90 % for a wide range of

supply voltage. Hence, the voltage drop across the control device can be reduced, and therefore the efficiency is improved.



(A) (B)

FIGURE 1.1: Linear (a) and switching (b) regulators.

Switching regulators present higher efficiency than linear regulators because their active devices operate as switches to perform power conversion, and therefore are not required to operate in active region.

For a switching regulator, there is also a feedback loop to regulate the output voltage to the desired voltage. Whenever the output voltage is not the expected, the feedback controller will decide to charge or discharge the energy store component by modulating the pulse width or frequency [6].

They have important disadvantages that make them useless for some applications. The dynamic response can be affected by its limited bandwidth, the output ripple is large because of the switching activities and usually the cost is higher due to off-chip components.

Next table 1.1 compares the general characteristics of linear and switching regulators.

	Linear regulator	**Switching regulator**
Function	$Vout < Vin$	$Vout < Vin$ or $Vout > Vin$
Efficiency	Low	High
Cost	Low	High
Ripple/Noise	Small	Large
Dynamic response	Fast	Slow

TABLE 1.1: Comparison between linear and switching regulators.

1.2 Motivation

LDO have been one of the most important block in Power Management Unit. They have been used where a stable voltage supply must be guaranteed regardless of any changes in the current load and the input supply. As the market trend is to reduce the area of both the die and the board as much as possible, new fabrication processes are appearing reducing the dimensions (nano-scale) which allows the electronic industry demand the same results but inside a much smaller package. Therefore, output capacitorless LDOs (CL-LDO) became a very promising research topic.

As the SoC products are more and more popular recently, CL-LDO becomes indispensable, since the analog circuits must be protected from the noise generated by the switching of the digital signals.

Low power consumption is a very critical requirement, especially in portable devices such as smart-phones and tablet PCs, since it determines the battery life. However, the CL-LDO regulators suffer from trade-off problem between power consumption and dynamic performance as well as stability.

1.3 Objectives

The purpose of this thesis is focused on the realization of an ultra-low power capacitorless LDO that presents frequency stability for a wide range of load conditions and fast dynamic response. Thus, several techniques of the State-of-the-Art for this kind of circuit were studied, analyzed and used.

The LDO must be fully integrated on-chip, which means that no external capacitor can be used to set the dominant pole and to avoid output voltage changes during load current transitions. This makes the design particularly challenging, specially when compared to conventional LDO solutions with external caps.

The design is implemented in Taiwan Semiconductor Manufacturing Company (TSMC) $40nm$ Low Power (LP) CMOS technology. This technology offers LVT, HVT, and SVT cells:

- HVT $\Rightarrow$ High Threshold Voltage: It is used in power critical functions. It offers less power consumption and the switching timing is not optimized.
- LHT $\Rightarrow$ Low Threshold Voltage: It is used in speed critical functions. It causes more power consumption and the switching timing is optimized.
- SHT $\Rightarrow$ Standard Threshold Voltage: It offers trade-off between HVT and LVT.

Furthermore, this process offers high-resistivity poly resistor and high density MOM [1] capacitor.

The software used for designing the CL-LDO was Cadence Virtuoso Custom IC Design. Matlab were also used to obtain some theoretical results.

The performance characteristics of the CL-LDO are summarized in table **??**. The specification for current consumption of this circuit at no-load condition is $900nA$. Although this value is variable in a range of $900nA$ to $90\mu A$, it is directly correlated with the load current consumption to ensure a high power efficiency of the system.

[1] Metal Oxide Metal (MOM) capacitors are implemented using the parasitic capacitance between two conductors on a metal layer. Several metal layers are connected in parallel by vias, forming a vertical metal wall or mesh which increases the capacitance density (capacitance per unit area of silicon chip)[1]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{IN}	1.33	1.4	1.47	V
Output voltage	V_{OUT}	-	1	-	V
Drop-out voltage	V_{DO}	-	400	-	mV
Quiescent current	I_Q	-	900	-	nA
Load current	I_L	0	-	100	mA
Edge time	$t_{rise/fall}$	0	300	-	ns
Current pulse width	$I_{L_{width}}$	–	20	–	μs
Output capacitor	C_L	-	100	500	pF
Load transient regulation	$\Delta V_{OUT} + \Delta V_{OS}$	-7	-	$+7$	%
Phase margin	PM	45	-	-	$^\circ$
Gain margin	GM	10	-	-	dB

TABLE 1.2: Performance Characteristics of the CL-LDO.

1.4 Structure of the Work

This thesis is organized in 6 chapters.

- Chapter 2: Low Drop Out (LDO) Voltage Regulator

This chapter presents the conventional LDO, discusses the structure as well as the general design considerations. It also presents the fully integrated LDO as an improvement.

- Chapter 3: State-of-the-art CapacitorLess LDO

The main published compensation and circuit techniques to improve the performance concerning capacitorless LDOs are described and compared in this chapter.

- Chapter 4: Circuit techniques for improved CL-LDO performance

In this chapter some of the state-of-the-art techniques are simulated and analysed in detail. First, a basic CL-LDO with miller compensation is shown. Then, few circuit techniques are added and analysed one-by-one to understand how they are affecting the overall performance. Finally, the chapter ends up with a proposed CL-LDO.

- Chapter 5: Proposed CL-LDO results

The performance evaluations based on detailed simulations of the proposed CL-LDO are presented.

- Chapter 6: Conclusions

Finally, this chapter presents conclusions as well as gives suggestions for future works.

Chapter 2

Low Drop Out (LDO) Voltage Regulator

2.1 Conventional LDO topology

Fig. 2.1 shows the architecture of a classical CMOS Low-Drop Out which is made-up of an error amplifier (EA), a feedback resistor network, a pass transistor, and a voltage reference. The Error amplifier is responsible of comparing the reference voltage with the output voltage obtained by the resistive feedback and also of driving the pass transistor in function of the comparison result. Assuming the voltage gain of the regulator is large enough, the output voltage is determined by the ratio of the output resistors R_1 and R_2, and by the voltage reference.

$$V_{OUT} = (1 + \frac{R1}{R2})V_{REF} \tag{2.1}$$

The pass transistor is a power device which controls the current flowing to the load. The structure needs to be compensated because it has two low-frequency poles, which are located at the output of LDO, and the output of the error amplifier, respectively. In order to source large output current without having a large voltage drop, the power transistor has to be very large compared to the internal transistors. Therefore, the equivalent parasitic capacitance at the gate of the power transistor is relatively large. Conventional LDOs make use of a large external capacitor to create the dominant pole. Furthermore, it provides an instantaneous charge during fast load transients [28].

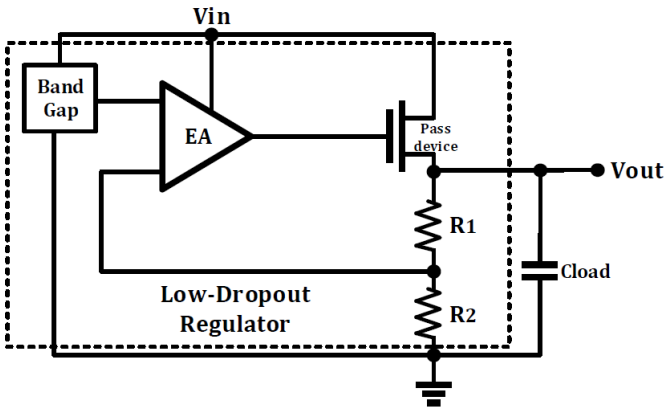


FIGURE 2.1: Typical linear voltage regulator topology.

2.2 Structure

2.2.1 Pass device

The output stage in linear regulators can be designed with different possible configurations depending on the circuit performance and power efficiency. One important criterion for the pass device selection is the drop-out voltage[1] from the input to the output voltage.

Fig. 2.2 shows different pass device topologies used in CMOS linear regulators: nMOS source follower, pMOS common source and native [2] transistor.

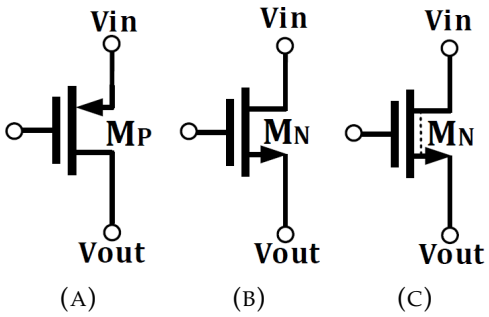


FIGURE 2.2: Pass device structures pMOS (a), nMOS (b), and native (c)

Generally, for the same size, nMOS transistor has higher current conduction ability due to the higher electrons mobility. However, in order to achieve low drop-out voltage, pMOS are preferred, despite their lower current conduction ability. Additionally, its gate voltage is always lower than the supply voltage.

On the contrary, in nMOS the gate voltage can be higher than the supply when is designed to operate in low drop-out voltage. Therefore, additional circuitry which brings more design complexity may be required. However, nMOS consumes smaller area for the same maximum current and provides better dynamic performance in large signal as the source node is directly connected to the output of the regulator. Hence, when the load current suddenly changes, e.g $I_{L_{min}}$ to $I_{L_{max}}$, $Vout$ decreases, and so Vgs quickly increases, thus regulating the pass device to drive $I_{L_{max}}$.

On the other hand, pMOS only needs a minimal drop-out voltage of $Vdsat$ in order to be fully saturated, while nMOS is saturated providing a minimal drop-out voltage $Vsat + Vgs$, unless the process offers nMOS transistors with zero threshold voltage. This type of transistors are called native or zero-Vt transistors.

The DC gain is also affected by the pass device architecture. With pMOS, the overall gain is increased because acts as second stage (common-source),

[1]The drop-out voltage is defined as the minimum voltage difference between the input supply V_{IN} and the output voltage V_{OUT} in order to maintain the regulation. It is directly related to the load current. The maximum drop-out voltage of an LDO is usually in the range of $200 - 600mV$ at full current load condition.

[2]Native MOSFET is a transistor where the threshold-adjust implant has been blocked (which requires additional mask). Therefore, they result in very low threshold voltage (sometimes negative). However, because of the extra dopping mask, the manufacturing cost is increased [42].

and therefore better steady-state regulation is achieved, as will be shown in the following of this Chapter. With nMOS, the DC gain is ideally not affected, since it acts as common-drain, and so the regulator will be easier to stabilize because the output resistance is much less instead.

2.2.2 Error amplifier

The error amplifier (EA) compares the reference voltage with the feedback voltage from the output and amplifies the difference. It is responsible of driving the gate of the pass device to the appropriate operating point to ensure that the output is at the correct voltage. As the current load and the power supply changes, the EA drives the pass device to maintain a constant output voltage. Therefore, the error amplifier design is crucial to ensure the driving requirements of the pass device and the performance of the system.

The main specifications for designing the error amplifier mainly are:

- High DC gain to ensure good line and load regulations. 2.3.4.1
- High bandwidth and high output current slew rate for responding to fast load transitions. 2.3.4.2
- Large output voltage swing for driving the pass devices under the whole current load and input voltage range.
- The topology is directly related to the overall power-supply rejection of the regulator. 2.3.1

Trade-off between quiescent current [3] and performance is therefore necessary.

2.2.3 Feedback Network

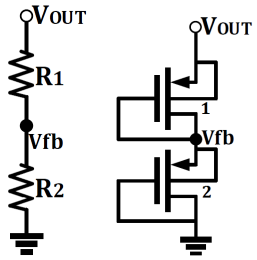
The feedback network can be realized by a string of diode-connected transistors or by a resistive network divider.

The use of the resistive network divider seen in Fig.2.3a allows high accuracy and robustness. First, the bigger the resistors are, the less will be the manufacturing variations. Second, resistors have less variations in the change of temperature. The drawback of using resistor is the extremely big area, especially when a low current consumption is required.

On the other hand, the use of diode-connected feedback network [9] [8] shown in Fig.2.3b allows an area decrease.

All the bodies of each transistor are connected to their source nodes, so that all have identical bias conditions. As the same current will flow through the transistors, the voltage Vfb can be easily fixed. For example, sizing the transistors identically, each transistor will drop the same voltage Vds (Vgs), since $I_{D_1} = I_{D_2}$. Hence, the voltage will divide evenly $Vfb = V_{OUT}/2$.

[3] The quiescent current is the difference between the input and the output current which does not contribute to the output power [15].



(A) Resistive (B) Diode-connected

FIGURE 2.3: Feedback network topologies.

2.3 Design considerations

A brief introduction of the design considerations for LDO regulators is introduced in this section. The key design considerations mainly are: stability at very light current loads, power-supply rejection, regulation performance as well as the efficiency. A special emphasis is made on the trade-off of these parameters.

2.3.1 Power-Supply Rejection

Power-supply rejection (PSR) is the ability to regulate the output against low and high-frequency small-signal variations in the power supply. PSR is highly related to line regulation since both refers to the ability of a LDO to regulate its output against variations in input supply. The difference is that line regulation only specifies the DC variations while PSR specifies a wide range of frequencies.

PSR is defined as the complement of supply injection, either as the reciprocal of supply gain Δ_{in}. The supply gain is referred to the small-signal variation in output voltage caused by small-signal variations in the input supply [28].

$$PSR = \frac{1}{\Delta_{in}} = \frac{\delta v_{in}}{\delta v_{out}} \tag{2.2}$$

As shown in 2.4 the noise coming from the input supply can couple to the output through several paths: through the voltage reference, the error amplifier and the pass device M_P. The contribution of supply noise coming from the path 1 (band-gap) usually is negligible. The ripple is minimum if a high PSR voltage reference is implemented. Otherwise, it can be easily reduced by adding a low-pass filter to the output of the voltage reference.

Basically, the PSR of the LDO strongly depends on the error amplifier and the pass devices topologies.

The concept to define the error amplifiers as Type-A and Type-B was introduced in [21] in order to analyze the PSR of the LDO. This concept is only valid for DC and low frequencies PSR. For high frequencies, the analysis are no longer valid, since it does not take into account the parasitics paths. However, it is useful to gain insight how the error amplifier architecture can affect the performance of the regulator in terms of PSR.

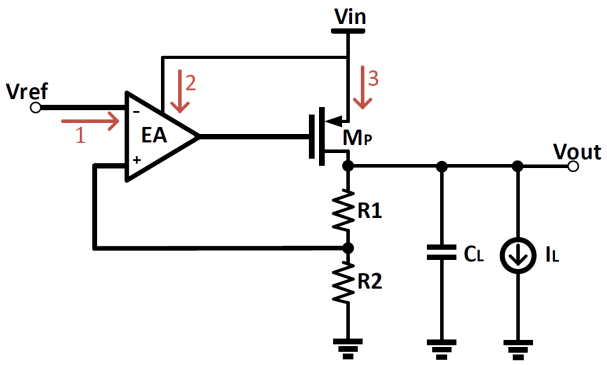


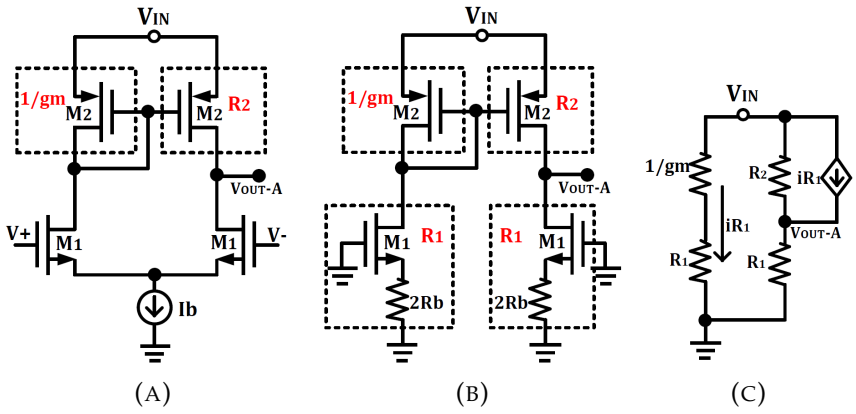
FIGURE 2.4: Coupling paths of supply noise to the output of the LDO.

Fig.2.5 show an example of a Type-A amplifier and the small-signal model for PSR of Type-A amplifiers. The Type-A consists of an nMOS input differential pair and a pMOS current mirror load. The model is obtained by applying an AC signal at the power supply Vin and grounding the inputs of the amplifier $V+$ and $V-$.

R_2 is the channel resistance of transistor M_2, and R_1 is the equivalent degenerated resistance, which is approximately equal to $gm_{M_1} rds_{M_1} 2R_b$, where resistor R_b represents the current source Ib small signal resistance, gm_{M_1}, and rds_{M_1} are the transconductance and the channel resistance of transistors M_1. Assuming $R_1 \gg 1/gm$, the current iR_1 can be approximate to Vin/R_1.

Next following equation 2.3 shows the derivation of the transfer-function $Vout_A/Vin$. Therefore, for Type-A amplifiers, the supply ripple is ideally transfered to the output.

$$V_{OUT_A} = Vin(\frac{R_1}{R_1+R_2}) + iR_1(R_1//R_2) \approx Vin(\frac{R_1}{R_1+R_2}) + \frac{Vin}{R_1}(\frac{R_1R_2}{R_1+R_2}) = Vin \tag{2.3}$$



(A) (B) (C)

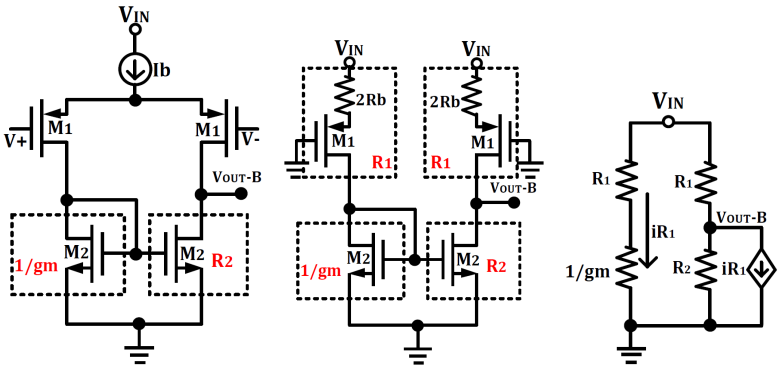
FIGURE 2.5: Type-A EA and its small-signal translations.

On the other hand, an example of Type-B amplifier and the small-signal for PSR of Type-B amplifiers are shown in Fig.2.6, respectively. The amplifier consists of a pMOS differential input pair and nMOS current-mirror.

The small-signal is obtained in the same way as Type-A, by applying an AC signal at the power supply Vin and grounding the inputs of the amplifier. The derivation of the transfer function $Vout_B/Vin$ is as follows:

$$V_{OUT_B} = Vin(\frac{R_2}{R_1+R_2}) - iR_1(R_1//R_2) \approx Vin(\frac{R_2}{R_1+R_2}) - \frac{Vin}{R_1}(\frac{R_1R_2}{R_1+R_2}) = 0 \tag{2.4}$$

As can be observed, ideally no AC ripple appears at the output. Thus, the output is isolated from the power supply.

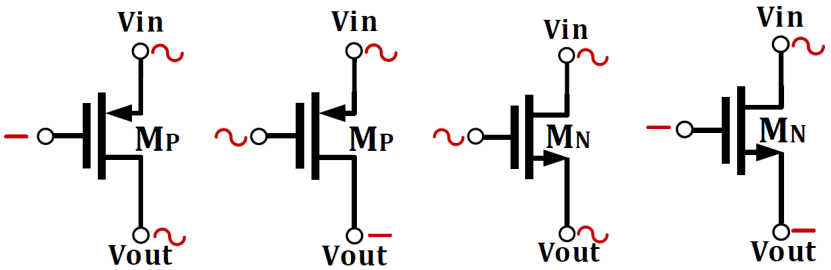


(A) (B) (C)

FIGURE 2.6: Type-B EA and its small-signal translations.

The pass transistor also has an important role in the PSR. For example, considering nMOS pass transistors, as shown in Fig. 2.7c and 2.7d, the nMOS will conduct the ripple present at its gate directly to the source; the output of the regulator. Therefore, to reduce the ripple at the output, it is crucial to design the error amplifier such that the ripple at the gate of the nMOS is the minimum possible (Type-B EA). In other words, gate-source (Vgs) should be common-mode with respect to each other.

pMOS pass transistors present the opposite scenario (Fig. 2.7a and 2.7b). To eliminate the supply ripple at the output, the gate of the pMOS should present the same ripple (Type-A EA) so that the gate is common-mode with respect to the source.



(A) pMOS (B) pMOS (C) nMOS (D) nMOS

FIGURE 2.7: Effects of common-mode signals on V_{OUT}.

Next table 2.1 summarizes how PSR is affected depending on what type of error amplifier (Type-A/B) and pass transistor (nMOS/pMOS) are used.

Error amplifier	Pass device	PSR
Type-A	pMOS	Better
Type-A	nMOS	Worse
Type-B	nMOS	Better
Type-B	pMOS	Worse

TABLE 2.1: PSR depending on error amplifier and pass device topologies.

2.3.2 Stability

Since the LDO regulator is based on negative feedback, it is very important to ensure the correct frequency behavior and so guarantee the closed-loop stability. The locations of the poles and the unity gain bandwidth (UGB) vary significantly with the load current condition.

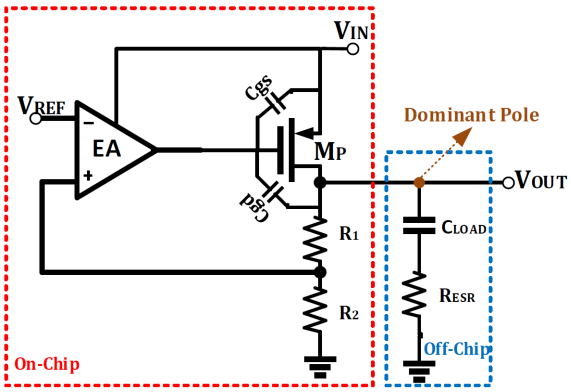


FIGURE 2.8: Conventional LDO regulator.

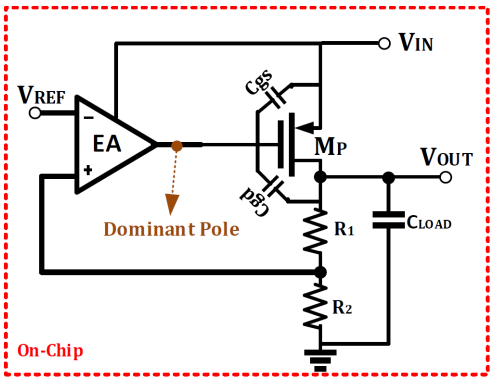


FIGURE 2.9: CL-LDO LDO regulator.

The compensation strategy would change depending on the size of the output capacitor: In conventional LDO (Fig. 2.8) the dominant pole is located at the output node. This is mainly because of the very large external capacitor and the high output impedance. Furthermore, a non-dominant pole is located at the gate of the pass device due to the high output impedance of the error amplifier and the parasitic capacitance Cgs and Cgd of the pass device. On the other hand, capacitor-less LDO shown in Fig.2.9, has the

dominant pole and non-dominant pole located at the gate of the pass device and the output node, respectively.

In both cases, these two low-frequency poles can be very close together. Therefore, external or internal compensation is required in order to guarantee the stability of both regulators. Usually, conventional LDO makes use of the equivalent series resistance R_{ESR} of the load capacitor to produce a LHP zero for compensating the phase shift introduced by the non-dominant pole [31].

As this thesis focusses on capacitor-less LDO regulators, their stability design considerations are explained in more detail in the following subsection 2.3.2.1.

2.3.2.1 CL-LDO Stability analysis

For stability analysis of the CL-LDO as well as for understanding how poles are moving as a function of the current load, the small-signal model shown in Fig. 2.10 has been built, where the feedback loop was broken for the purpose of the analysis.

The compensation capacitor C_M is used with the intention of causing pole-splitting and ensuring the non-dominant pole location at the output of the regulator. According to Miller effect, the dominant pole (node V_1) is moved to lower frequency and the non-dominant pole (output pole) is moved to higher frequency [33].

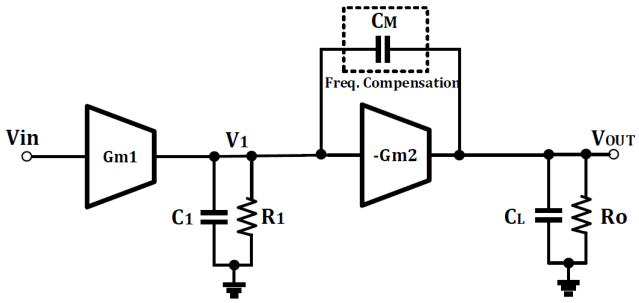


FIGURE 2.10: CL-LDO Small-signal model for stability analysis.

The nodal analysis can be done as shown below:

$$\begin{cases} vingm_1 + (vout - v_1)sC_M = v_1(sC_1 + \frac{1}{R_1}) \\ -v_1gm_2 + (v_1 - vout)sC_M = v_2(sC_L + \frac{1}{R_O}) \end{cases}$$

Where Gm_1 and Gm_2 are the transconductances of the error amplifier and the pass device, respectively. R_1 and R_O are the output resistance of the EA and pass device. Finally, C_1 and C_L are the capacitance associated with each node.

Solving the two equations system, the transfer function from $Vout$ to Vin can be expressed as follows:

$$\frac{Vout}{Vin} \approx -\frac{gm_1gm_2R_1R_O(1 - s\frac{C_M}{gm_2})}{1 + s(C_1 + C_Mgm_2R_O)R_1 + s^2\frac{(C_1+C_Mgm_2R_0)R_1(C_1+C_L)}{gm_2}} \tag{2.5}$$

The second order transfer function has two poles and a single right half plane (RHP) zero.

$$p_1 \approx -\frac{1}{(C_1 + C_M \Delta pass) R_1} \tag{2.6}$$

$$p_2 \approx -\frac{gm_2}{(C_1 + C_L)} \tag{2.7}$$

$$Z_1 = \frac{gm_2}{C_M} \tag{2.8}$$

Where Δ_{pass} is the gain of the second stage which is equal to the product $gm_2 R_O$.

As mentioned already at the beginning of this section, the pole frequency location is dependent on the current load condition. The small-signal parameters that change in function of the current load are related to the pass device: gm_2 and R_O. Fig. 2.11 shows the stability analysis under

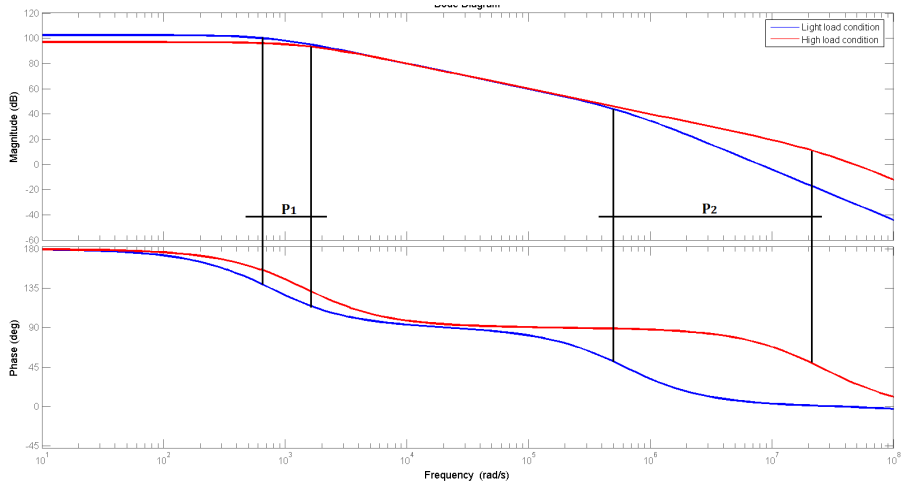


FIGURE 2.11: Bode of two-stage CL-LDO using the given pole/zero expressions in Matlab for light and high current load conditions.

light (blue) and high (red) current load conditions. The small-signal parameters were extracted from Cadence and then introduced in Matlab for better visualization. As can be observed, when the current load increases, the non-dominant pole p_2 moves to higher frequencies, while p_1 barely changes. Usually, at light load condition, the pass device is in sub-threshold operation (weak inversion [4]). This is because the pass transistor requires large W/L to drive large current loads.

In medium/high current load, pass transistor is operating in moderate/strong inversion. This change of operation (weak to moderate or strong) would move both pole p_1 and p_2 towards higher frequencies;

While the pass device is in weak inversion, p_1 would remain constant, since the product $gm_2 R_O$ is not ideally changing (see equations 2.9 and 2.11). However, in moderate/strong inversion it is moving in function of $\sqrt{I_{LOAD}}$. Besides, pole p_2 in weak inversion is varying in function of I_{LOAD},

[4]The weak inversion region or sub-threshold region is the zone where V_{GS} is well below threshold voltage. The gm/I_D ratio is higher compared to moderate/strong inversion.

while in moderate/strong in a function of $\sqrt{I_{LOAD}}$. Consequently, in the transition from weak to strong inversion, p_2 changes at a faster rate than p_1.

The following equations give the transconductances when the transistor is operating either in weak, or strong inversion inversion:

$$gm_{Weak} = \frac{I_D}{nU_t} \tag{2.9}$$

$$gm_{Strong} = \sqrt{2K\frac{W}{L}I_D} \tag{2.10}$$

Where U_t is the thermal voltage $U_t = kT/q$, and the slope factor $n = 1 + C_D/C_{OX}$.

The resistance changes at the same rate either in weak, or strong:

$$R = \frac{1}{I_D\lambda} \tag{2.11}$$

2.3.3 Efficiency

Efficiency is a very important parameter specially in portable systems since it determines the life time battery. The power efficiency of a LDO is the relationship between the output power and the power supply which is defined by the drop-out voltage, the load current, and the quiescent current. The relationship is shown in equation 2.12

$$\eta = \frac{V_{OUT}I_{LOAD}}{V_{IN}(I_{LOAD} + I_Q)} \tag{2.12}$$

Where V_{IN} and V_{OUT} are input and output voltages, respectively. I_Q is the quiescent current and I_{LOAD} the load current.

Two different situations can be identified for the analysis of power efficiency, one related to small load currents 2.13 and the other to large load currents 2.14.

Assuming $V_{OUT} \approx V_{IN}$, the relation reduces to equation 2.13 for small load current conditions ($I_{LOAD} \downarrow\downarrow$), thus the power efficiency is determined by the quiescent current itself. For portable devices this parameter is extremely important since if the current load is very low (Ex. stand-by operation) the longevity of the battery life will depend exclusively on the quiescent current consumed.

$$\eta_{LightILoad} \approx \frac{I_{LOAD}}{I_{LOAD} + I_Q} \tag{2.13}$$

In high load current condition the quiescent current is negligible compared with load current. Therefore, the efficiency is determined by:

$$\eta_{HeavyILoad} \approx \frac{V_{OUT}}{V_{IN}} \tag{2.14}$$

2.3.4 Regulating performance

The voltage regulator performance can be divided into steady-state regulation and the dynamic regulation.

The steady-state regulation is mainly affected by the loop-gain of the LDO. The dynamic performance is the most challenging parameter of the LDO, specially for the capacitor-less which goes without the large output capacitor.

2.3.4.1 Steady-state

The steady-state parameters include the load regulation and the line regulation. They are normally defined for a given LDO regulator, and measure the capability to regulate the steady-state output voltage for given line and load steady-state values.

2.3.4.1.1 Load regulation The load regulation is the capability of the regulator to maintain the output voltage with steady state variations in load current. It is measured when the output voltage is in steady state. It depends on the LDO output resistance R_{OL} and the LDO open-loop gain R_{OL}.

$$Load\ regulation = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{OL}}{1 + A_{OL}R_{OL}} \tag{2.15}$$

Therefore, a load current change is equivalent to the closed loop output resistance of the regulator thus the higher the DC gain, the better the load regulation.

2.3.4.1.2 Line regulation Line regulation defines the ratio of the output variation change in response to a variation in the input voltage after the regulator has reached the steady state. It depends on the pass device transconductance, g_{mp}, the LDO output resistance R_{OL}, the LDO open-loop gain R_{OL} and the feedback gain β.

$$Line\ regulation = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{g_{mp}R_{OL}}{A_{OL}} + \frac{1}{\beta}(\frac{\Delta V_{REF}}{\Delta V_{IN}}) \tag{2.16}$$

2.3.4.2 Dynamic-state

As the main purpose of this thesis is to improve the transient response of the capacitor-less LDOs, the next chapters will constantly mention the concepts presented in the following of this subsection.

The dynamic-state specify the ability of the LDO to regulate the output voltage during load transient transitions. Responding to a load transient becomes challenging when the load current steps are very fast. This is common for digital circuits where clock speeds are high and the circuits have large logical functionalities. Responding to a current change with a rise and fall times of several nanoseconds requires a very fast response (bandwidth) from the regulator which is not achievable for very low quiescent current. Hence, these current transitions are outside of the time response and the regulator cannot react to the load change.

Fig. 2.12 illustrates a typical output response to a worst-case load current variation, when the load current suddenly transitions from its highest value to its lower value, and vice versa. The capability of the regulator to respond to these fast current load transitions will depend on the current-load, the output capacitor, and the LDO response time. The output voltage

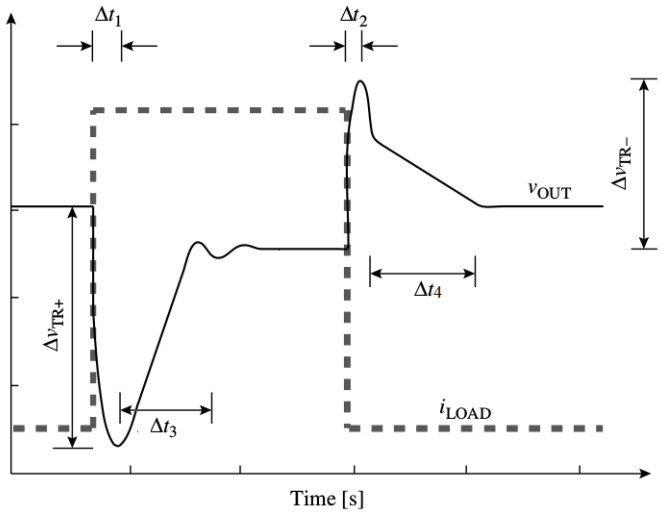


FIGURE 2.12: Typical transient response to abrupt load current changes [29].

variation is given in 2.17.

$$\Delta V_{OUT} = \frac{I_{MAX}\Delta tr}{C_{OUT}} \tag{2.17}$$

Where I_{MAX} is the maximum output current, C_{OUT} is the output capacitor and Δtr is the regulator response time. As seen, ΔV_{OUT} is inversely proportional to C_{OUT}. Conventional LDO topologies make use of a large capacitor at the output in parallel to the load. The purpose of this large capacitor is to act like a charge source during fast load current transitions and so improve the output voltage change of the regulator in addition to its AC stability [28]. Therefore, they will present better load regulation compared to capacitor-less LDO regulators.

The response time Δtr (Δtr_1, Δtr_2) is affected by the closed-loop bandwidth and also by the internal slew-rate due to the parasitic capacitors which cause slewing effects that degrade the regulator's load response.

$$\Delta tr = t_{BW} + t_{SR} = \frac{2.2}{BW} + C_{pass}\frac{\Delta V_{pass}}{I_{SR}} \tag{2.18}$$

Where t_{SR} is the slew rate time, $\frac{2.2}{BW}$ is the bandwidth delay time, C_{pass} is the parasitic capacitance at the gate of the pass device, and I_{SR} is the current driving the C_{pass}. The value of C_{pass} is mainly due to the gate capacitance of the pass device since the transistor is designed to have low voltage drop at maximum load current, i.e., the transistor size can be very large, thus capacitance C_{GD} and C_{GS} are usually large.

In the case of a positive load current transition (I_{LOAD} suddenly increase), the settling-time (Δtr_3) is dependent on the time required for the error amplifier to fully discharge the equivalent capacitance C_{pass} and the phase-margin of the loop frequency response. Usually the settling-time of the overshoot (Δtr_4) is larger compared to the undershoot. This is mainly because when a fast negative load current step occurs, the regulator takes

some time to react (Δtr_2), and meanwhile the pass device keeps sourcing current which charges the output capacitor C_L. Once the regulator responds, the pass device stop sourcing current. However, as the output capacitor is charged due to the slowness of the regulator, the output voltage may not return back to its targeted voltage until it does not fully discharge. As a consequence, the settling time would depend on the sinking capabilities the regulator has in order to discharge and slew the output capacitor.

The following Chapter 3 is presenting different techniques found during the State-Of-The-Art research to improve the dynamic performance of Capacitor-Less LDO without having too much impact on the area and the efficiency.

Derivation of $\frac{2.2}{BW}$ expression.
The rise time is defined as the time for the output to rise from 10% to 90% of the time step. Using the general step response 2.19 expression for the specific times $t_{10\%}$ to $t_{90\%}$.

$$V(t) = V_{OUT}(1 - e^{-\frac{t}{\tau}}) \tag{2.19}$$

$$0.1 = 1 - e^{-\frac{t_{10\%}}{\tau}} \tag{2.20}$$

$$0.9 = 1 - e^{-\frac{t_{90\%}}{\tau}} \tag{2.21}$$

$$t_{rise} = t_{90\%} - t_{10\%} = 2.2\tau \tag{2.22}$$

So, for the output voltage to reach 90 percent of its final value, 2.2 time constants $R_{OUT}C_{OUT}$ must elapse:

$$t_{BW} = 2.2RC = \frac{2.2}{2\pi f_{-3dB}} \tag{2.23}$$

Chapter 3

State-Of-The-Art CapacitorLess LDO

The focus of this thesis focusses on capacitor-less LDO, from now referred to as CL-LDO's, so an examination of the recent existing works related to this field is crucial to better understand their trade-offs.

Removing the large capacitor and replacing it by one smaller (in the range of few hundreds of picofarad), while having very small quiescent current as well as ensuring fast transient responses with good regulation is the most difficult design challenge for CL-LDO. Many researchers have been developing different techniques and topologies which improve considerably the performance of these LDO's without having too much impact on the area and efficiency. Thanks to them it is now possible to use ultra-low power CL-LDO voltage regulators totally integrated in a System-On-Chip having the desired results under fast transient variations without stability degradation.

In this section the most recent techniques to improve the CL-LDO performance are presented. A brief description is also presented for each technique including their most important trade-offs. This section ends up with a comparison table between the most recent works to have a better overview of the State-Of-The-Art.

3.1 Load transient topologies

3.1.1 Capacitive-coupling

The works in [2, 13, 23, 31] overcome the load transient and AC stability issues by employing an auxiliary fast loop (differentiator) which consists of a current amplifier in series with a capacitor Cf, as shown in Fig. 3.1. The Capacitor Cf responds to any output voltage change in the form of current, then this current is amplified by means of a current amplifier and it is injected to the gate capacitance of the pass device. Therefore, the transient response is improved. Moreover, the auxiliary loop splits the poles, similarly to [5] [27], improving the AC stability. However, this method requires extra capacitors and resistors, resulting in an increase in the chip area.

3.1.2 Adaptive Biasing Loop

Adaptive biasing, which increases the bias current according to the magnitude of load current is employed in [18, 43, 44]. This loop is used to adjust

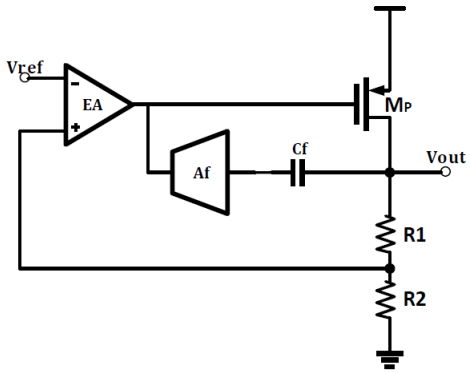


FIGURE 3.1: Differentiator architecture.

the bias current of the error amplifier according to the load current. Therefore, the bandwidth and the slew-rate current increases as the current load increases.

As shown in Fig.3.2, in addition to the small fixed $Ibias$ current, the EA is also biased with an extra adaptive bias current Iab proportional to the load current. This auxiliary loop is formed by the current sensing transistor M_{abl1} and a current mirror formed by transistors M_{abl2} and M_{abl3} which mirrors the small fraction of the load current into the EA. In low load conditions, the extra current injected to the error amplifier is negligible. On the other hand, at medium and heavy load currents the extra current is significant, resulting in an increase of the bandwidth and slew rate of the EA. As current Iab is a smaller fraction of the current load, the current efficiency is hardly affected.

$$\eta = \frac{V_{OUT} I_{LOAD}}{V_{IN}(I_{LOAD} + I_{BIAS} + I_{AB})} \tag{3.1}$$

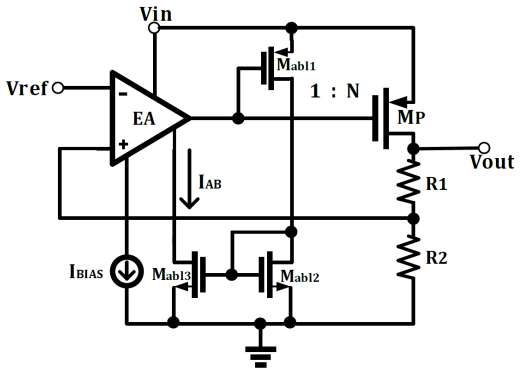


FIGURE 3.2: Adaptive Biasing Loop architecture.

The adaptive biasing current may need extra circuitry in order to accurately control the desired value. The power device M_P may enter triode region [1] for example, in the case the input voltage is reduced to the regulated output voltage $Vin = Vout$. As a consequence, the mirrored current

[1] Triode region, linear region or ohmic region: $V_{GS} > V_{Th}$ and $V_{DS} < V_{GS} - V_{Th}$. The amount of current which passes through the MOSFET will strongly depend on drain-source

may be very high as it is highly dependent on the V_{DS} matching.

In [29] they propose a current replica mirror that ensures that both M_{abl1} and M_P are in the same region of operation (Vgs and Vds for both devices are equal). The principle is to sense the voltage at the output terminal (drain of M_P) and force that voltage onto the drain of M_{abl1}. Therefore, if the pass device enters triode region, transistor M_{abl1} will be forced to operate in triode region as well.

3.1.3 High Slew-Rate Error Amplifier

Architectures in [3, 14, 38, 39] are using a current-mode error amplifier instead of a voltage-mode to improve the transient response. It is based on a Class-AB current-mode transconductance amplifier (CTA) to sink and source more current for discharging and charging the gate capacitance of the pass device during a load transient transition. When an error between the voltage reference and the output voltage is sensed, the CTA generates a current in order to sink or source the gate capacitance of the pass device.

However, there is an important trade-off between AC stability and slew rate; in order to maintain the stability at light load, the size of the transistors driving the pass device is relatively small, and could not sink or source the expected current to push up or pull down the gate voltage of pass device immediately. Hence, the large overshoot and undershoot may not meet the specification in some applications.

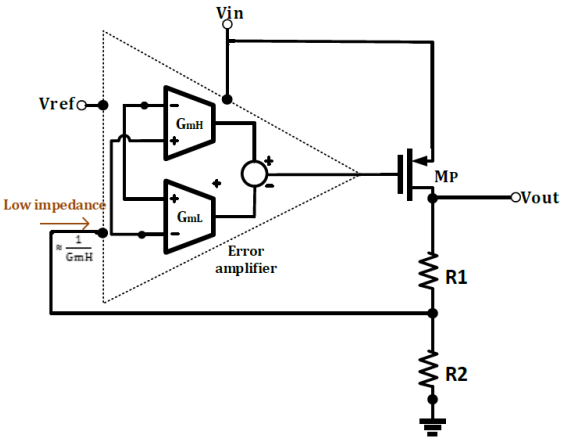


FIGURE 3.3: High Slew-Rate Error Amplifier architecture.

3.1.4 Push-Pull composite power transistor

The work in [11] uses a push-pull composite power transistor to enhance the slew-rate limitation at the gate of the power transistor M_{P1}. In addition, the non-dominant poles are pushed to higher frequencies, ensuring the stability. During a load current transition the push-pull structure will provide extra dynamic current at the gate of the pass device.

voltage. The transistor operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The drain current can be modeled as: $I_D = \mu C_{OX} \frac{W}{L}((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2})$

It works in a similar way than the High Slew-Rate EA topology. When an undershoot appears at the output due to a sudden increase in the load current, V_{OUT} drops quickly, this drop is then sensed by the EA. This drop will force the transistors M_2 and M_5 to be in off and on, respectively. Therefore, the gate of the pass device M_{P1} is discharged by M_5, allowing the pass device to conduct the current load. On the other hand, during an output overshoot transition, transistors M_2 and M_5 will turn on and off, respectively. Hence, M_2 injects current to the gate of the pass device, causing the pass device to turn-off to decrease the current load. However, it consumes high quiescent current in order to guarantee the stability.

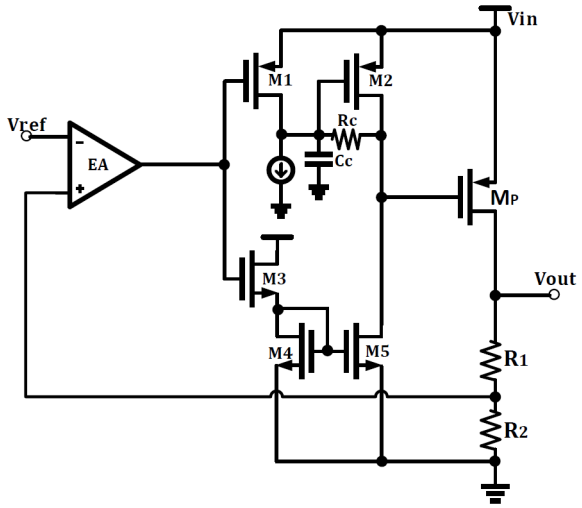


FIGURE 3.4: Push-Pull composite power transistor architecture [11].

3.1.5 Adaptive Power Transistor

Adaptive power transistor is a circuit technique that allows the regulator transforms itself from two stage to three stage and vice versa depending on the current load. At light load the regulator is working in two stage mode, both the second stage and main power transistor M_{P2} are turned off and the small sub-power transistor M_{P1} acts as a pass device. As load current increases, M_{P2} is turned on by the second stage which is also acting as a current comparator, and starts to deliver I_L to output, then the regulator transforms to three stage form. As a result, the gain of the CL-LDO is increased, and so the load and line regulation are improved, see equations 2.15 and 2.16. Conclusively, moving between two and three stage as a function of the current load allows improving the load and line regulation without stability problems. Furthermore, the area of sub-power transistor M_{P1} may be much less compared to the main power transistor M_{P2}, since it is designed to drive light current loads instead. Therefore, the equivalent gate capacitance at the gate of the pass device M_{P1} is greatly reduced, and so the regulator's time response is much less for driving the pass device M_{P1}.

This thesis is based on this circuit technique which is presented in [9]. Therefore, it will be explained in more detail in the next following Chapter 4 and 5.

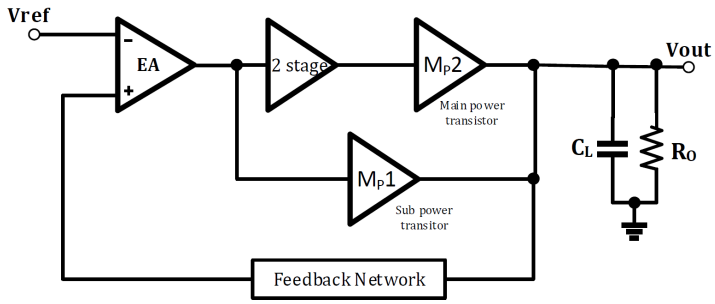


FIGURE 3.5: Adaptive Power Transistor architecture.

3.2 Compensation techniques

3.2.1 Q-Reduction

When removing the large external capacitor and maintaining the low power requirements, the non-dominant poles suffer changes thus producing high quality factor (Q) and non-dominant poles locations closer to the GBW.

The works in [32][44] use the Q-reduction architecture. This technique is used to generate non-dominant complex poles that are not directly correlated to the output load.

The structure is composed of three stages; a differential stage, a non-inverting gain stage and the pass device, respectively. Furthermore, it uses a Miller compensation capacitor $Cm1$ to have pole-splitting effect.

The current buffer in the first stage formed by transistors M_3 and M_4 together with the capacitor Ccf generate a feed-forward path between the output of the first stage and the output of the second stage that allows reducing the Q value of the non-dominant poles. Then, the quality factor will highly depend on the value of Ccf and the transconductance, the input resistance, and the input capacitance of the current buffer, making it easier to achieve lower Q-factor.

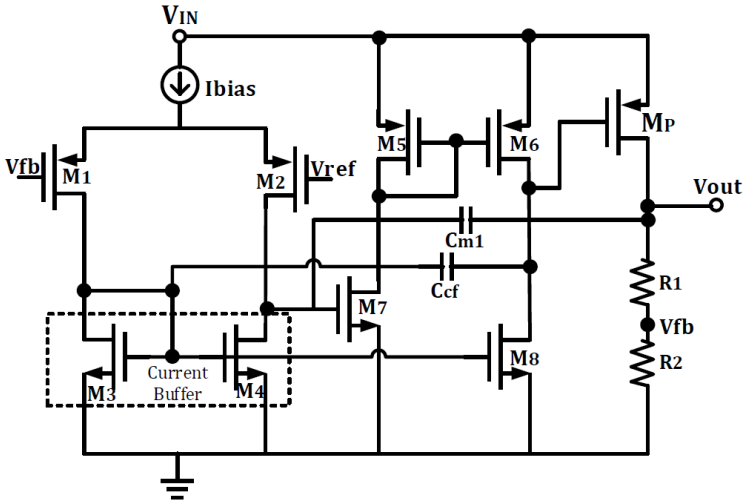


FIGURE 3.6: Q-reduction architecture [32].

3.3 Comparison of recent works

The next table 3.1 summarizes the state-of-the-art of the most recent works based on CL-LDO's to give a better overview of the characteristics and trade-offs of each work. It also includes two figures of merit (FOM) [41] for each work to have a better comparison between them.

FOM_1 is used for emphasizing the importance of the recovery time. It evaluates the effect of the quiescent current to the load transient response.

$$FOM_1 = TR\frac{I_Q}{I_{MAX}} = \frac{\Delta VoutCoutI_Q}{I_{MAX}^2}\ [s] \tag{3.2}$$

Where $\Delta Vout$ is the highest voltage spike due to a load transition, I_{MAX} is the maximum output load current, I_Q is the quiescent current, and TR is the response time, given as:

$$TR = \frac{Cout\Delta Vout}{I_{MAX}} \tag{3.3}$$

FOM_2 is used for emphasizing the importance of the load transient $\Delta Vout$.

$$FOM_2 = K\frac{\Delta VoutI_Q}{I_{MAX}}\ [V] \tag{3.4}$$

Where K is the edge rise/fall time defined by

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among designs for comparison}} \tag{3.5}$$

Note that a lower FOM implies a better overall performance. Lower FOM is achieved when the load capacitance, the quiescent current, the highest voltage spike and the edge time are lows, while supplying high currents load.

As seen in next Table 3.1 the works that make use of latest CMOS technologies present the better performance. This is mainly because the reduction of the dimensions of transistors leads to parasitic capacitance decrease, specially for the equivalent capacitance at the gate of the pass device which strongly affects the dynamic performance.

The work in [9] (Adaptive power transistor technique), presents the better load transient response (FOM_1, FOM_2) in much difference, even compared to [11] which is using the same technology $65nm$.

Works [10] [38] have the faster settling-time t_{settle}. However, they need minimum current load $I_{LOAD_{min}}$ to ensure the stability, as well as they have large output variations under load current transitions. The other works have very large quiescent current between $20\mu A$ and $30\mu A$ which are not suitable for ultra-low power applications.

Work	[24]	[13]	[7]	[43]	[40]	[38]	[24]	[11]	[9]	[40]	[17]
$Year$	2015	2010	2013	2011	2013	2012	2013	2014	2013	2015	2013
$Technology$	0.35	0.35	0.35	0.35	0.35	0.35	0.5	0.065	0.065	0.13	0.11
$Pass\ device$	CS	CS	CS	CS	CS	CS	CS	CS	CS	CS	CS
$V_{IN}(V)$	2	1.8-4.5	1.28-3.3	1.2	-	2.5-4	2-2.8	0.75-1.2	1.2	1	1.8-3.8
$V_{OUT}(V)$	1.8	1.6	1.1	1	1	2.35	1.5	0.5	1	0.8	2
$V_{DO}(mV)$	200	200	180	200	200	150	120	200	200	200	-
$\Delta V_{OUT}(mV)$	200	98	80	105	475	455	585	103	68	120	385
$I_{LOADmax}(mA)$	100	100	100	100	100	100	50	50	100	100	200
$I_{LOADmin}(\mu A)$	0	0	0	0	100	50	1	0	0	1	0.5
$I_{Quiescent}(\mu A)$	22	20	25	28	1.2	7	5.34	16.2	0.9	2.9	41.5
$C_{OUT}(pF)$	100	100	100	100	100	100	100	100	100	100	40
$t_{rise}(\mu s)$	1	2.5	0.5	1	1	0.15	0.1	0.1	0.3	0.8	0.5
$t_{settle}(\mu s)$	8.5	9	2	5	2.7	0.5	5	1.2	6	1.7	0.6
$Chip\ area(mm^2)$	0.182	0.145	0.126	0.0987	0.04	0.064	0.175	0.0096	0.017	0.042	0.21
$FOM_1(ps)$	0.044	0.02	0.02	0.029	0.006	0.0312	0.125	0.067	0.0006	0.0035	0.016
$FOM_2(mV)$	0.44	0.49	0.1	0.294	0.057	0.048	0.063	0.033	0.002	0.028	0.399

TABLE 3.1: State-Of-The-Art table comparison.

Chapter 4

Circuit techniques for improved CL-LDO performance

This chapter will analyze the performance improvement provided by different circuit techniques, when implemented in a state-of-the-art $40nm$ microelectronic technology. The study will begin with a basic CL-LDO design. Then, circuit techniques will be added and compared one-by-one to understand how they are affecting the performance of the system. The circuit techniques that will be analyzed are:

- Cascode compensation
- Adaptive biasing loop
- Adaptive power transistor
- Capacitive-coupling
- Gm-Boost

In each topology the load transient response is evaluated, when the output current switches between 0 to $100mA$ and vice versa within 300-ns edge time (i.e., the rise and fall time taken for the change of I_L). The regulated output voltage, the quiescent current and load capacitor C_{load} used for comparison are: $1V$, $900nA$, and $100pF$, respectively. Furthermore, in order to minimize the parasitic capacitance as much as possible, the transistors used for the design are thin gate oxide. Finally, the input voltage is $1.8V$, this is because the first topologies do not respond pretty well to load current transitions and with a high input voltage it can be seen how far the output voltage can get.

4.1 Basic CL-LDO architecture Miller compensation

Next Fig. 4.1 illustrates the architecture of the proposed basic CL-LDO. It consists of a nMOS differential pair as error amplifier, a pMOS pass device, and a resistive feedback network.
The regulator is being stabilized by using Miller compensation, comprising a local capacitor C_M. The stability analysis is the same as that already presented in Chapter 2.

In addition, the capacitor C_M may reduce the time response of the LDO, as it creates a path between the output and the gate of the pass device V_{pass}

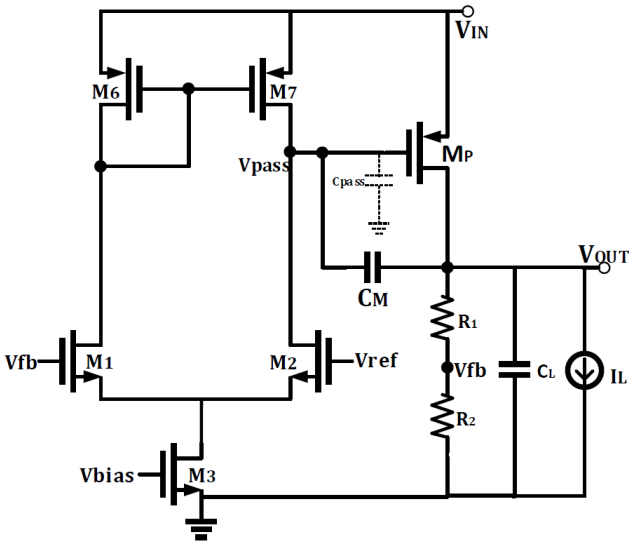


FIGURE 4.1: Schematic view of basic CL-LDO: Miller compensation.

(in a similar way to 3.1.1), sensing any change in voltage difference between these two nodes, and generating a proportional current to the change in the output voltage:

$$I_{C_M} = C_M \frac{d(V_{pass} - V_{OUT})}{dt} \tag{4.1}$$

This current is bi-directional, responding to a positive or negative change in output voltage.

While this C_M has the positive effect of adding a fast path between the output and the gate of the pass device, it also increases the equivalent capacitance $Cpass$ due to the Miller effect. Therefore, the addition of C_M produces the complementary effects of higher slew-rate current and higher parasitic capacitance $Cpass$. In addition, higher values of C_M may reduce the gain-bandwidth, since it is inversely proportional to C_M:

$$GBW = \beta g m_1 / C_M \tag{4.2}$$

Note that the fast path benefit described before will be irrelevant if the bias current of the error amplifier is large enough to provide driving currents much larger than those across C_M. But in that situation, the increased $Cpass$ capacitance because of the Miller effect and the decreased bandwidth will persist, thus degrading the time response of the error amplifier.

Next Fig. 4.2 shows the load transient response obtained for different values of C_M. Clearly, the large output voltage spikes are unacceptable. The output voltage approaches zero volts and V_{DD} for any value of C_M. Fig. 4.3 shows a zoomed-in view of the undershoot transition, the current I_{C_M}, the EA slew-rate current (drain of M_2), and the load current transition, respectively. Note that the increase in C_M affects not only the magnitude of the undershoot but also the settling-time. The reduction in magnitude is due to the higher current spike (I_{C_M}) injected at the gate of the pass device that discharges the equivalent capacitance C_{pass} until the output voltage

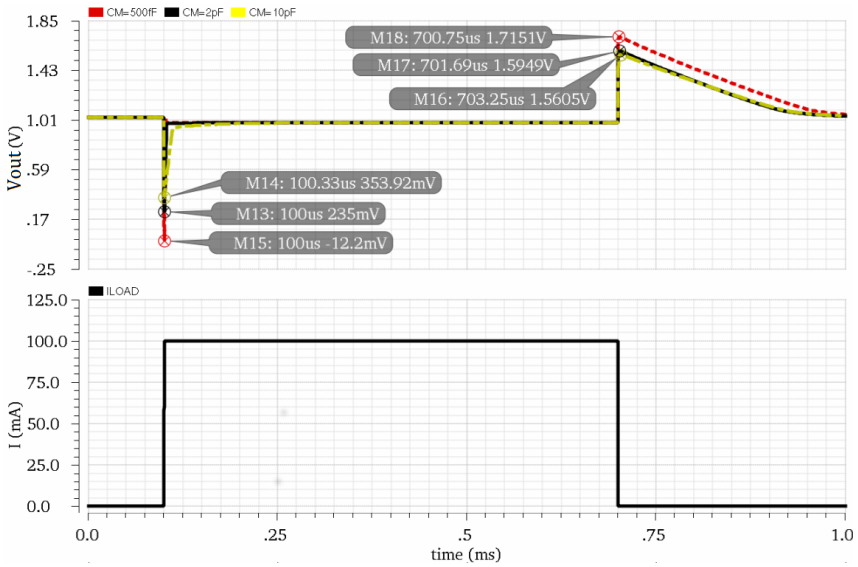


FIGURE 4.2: Dynamic response: $C_M = 500fF$ (dotted-red), $2pF$ (black), and $10pF$ (dashed-yellow).

stops lowering, at this moment, the injected current will rapidly decrease down to zero (Eq. 4.1). On the other hand, the larger the gate capacitance (C_{pass} proportional to C_M because of Miller effect) the larger the propagation delay will be (settling-time).

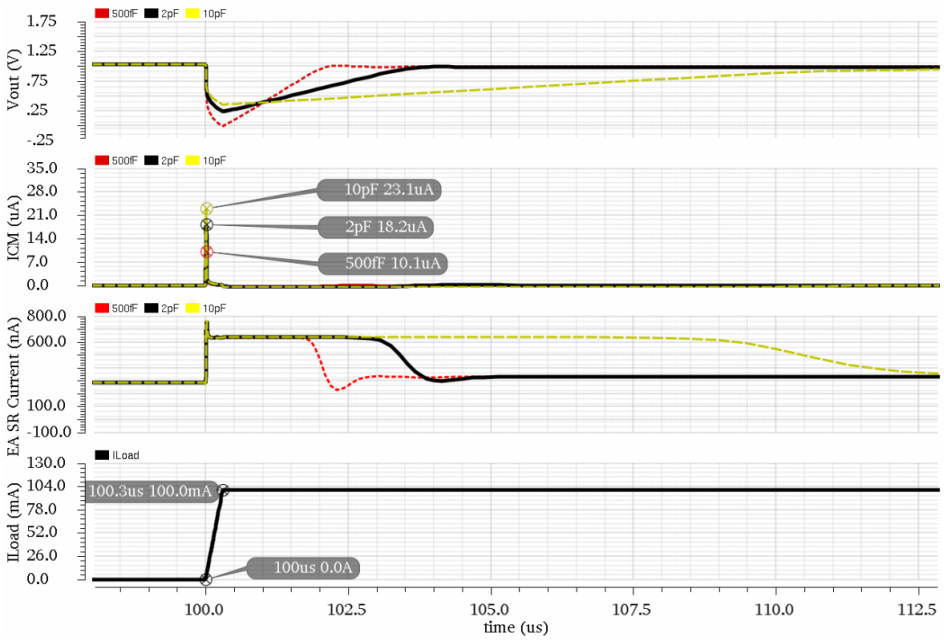


FIGURE 4.3: Undershoot transition: $C_M = 500fF$ (dotted-red), $2pF$ (black), and $10pF$ (dashed-yellow).

The settling-time of the overshoot transition is barely affected by the variation in capacitor C_M. As already commented in 2.3.4.2, the settling-time will depend on the sinking capabilities the regulator has in order to

discharge and slew the output capacitor. In this particular case, the only path to discharge it is through the feedback network which consumes $250nA$ of quiescent current. The following Fig. 4.4 compares the settling-time for different values of quiescent current in the resistive feedback network; $250nA$ and $1\mu A$. The figure also includes the charging/discharging current of the output capacitor C_L for better visualization. As expected, the output capacitor discharges faster when the regulator has more sinking capabilities.

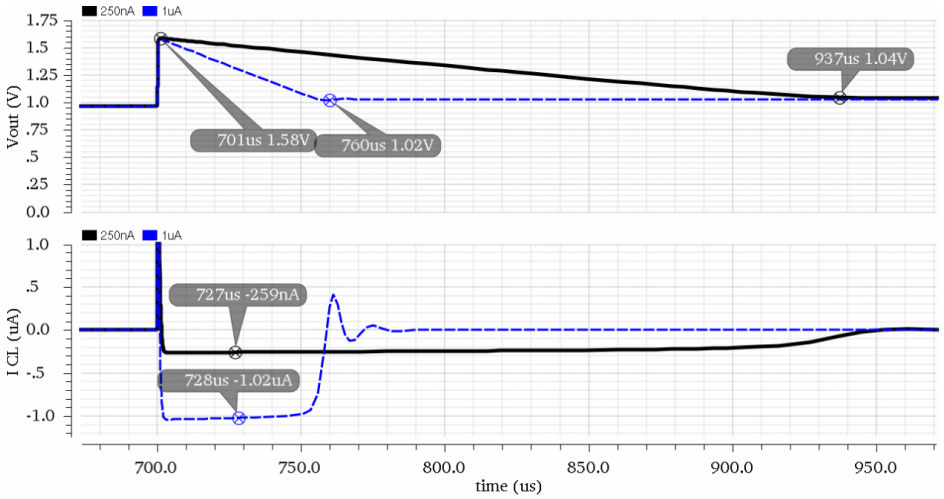


FIGURE 4.4: Overshoot settling-time comparison (2pF) with $250nA$ (black) and $1\mu A$ (dotted-blue) discharging current.

4.2 Cascode compensation

One solution that improves the trade-offs described for the Miller compensation is to add a series current buffer. A simple way to implement the current buffer is by using a cascode stage (telescopic amplifier), as seen in Figure 4.5, where transistor M_5 acts as a common-gate. Telescopic architecture is preferred instead of Folded Cascode, since it requires less quiescent current for the same EA slew-rate current. However it may not be useful for some low power applications, due to higher overhead voltage. It can be compared with the architecture presented in section 3.1.1, but here the current buffer is embedded into the error amplifier. Unlike Miller compensation, the compensation capacitor is isolated from the gate of the pass device V_{pass} by means of the current buffer. In consequence, the equivalent capacitance C_{pass} is ideally not affected by C_C. Furthermore, as shown in the small-signal analysis below , it provides more pole-splitting and better stability response compared to Miller compensation, since it creates a LHP zero instead of a RHP.

Same as with Miller compensation, the compensation capacitor C_C senses any change in voltage difference between V_{OUT} and V_C, generating a proportional current to the change in the output voltage.

$$I_{C_C} = C_C \frac{d(V_C - V_{OUT})}{dt} \tag{4.3}$$

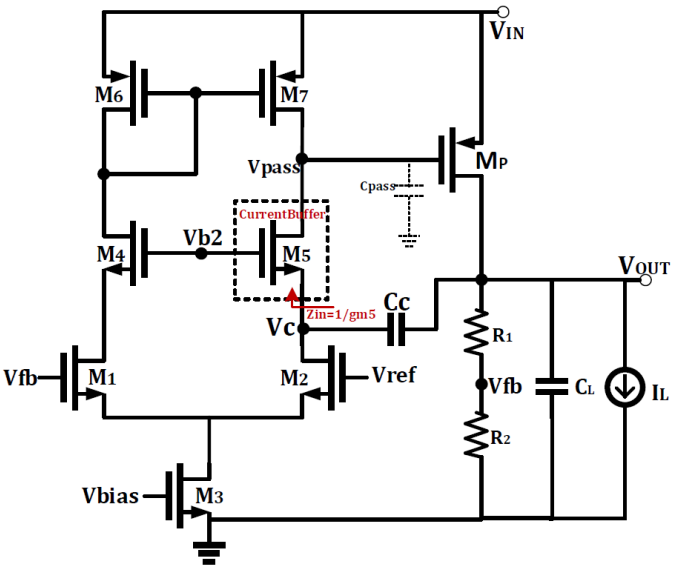


FIGURE 4.5: Schematic view of cascode compensation.

However, due to the current buffer, this current is unidirectional, responding only to a negative output voltage.
During a negative output voltage, the current I_{C_C} will attempt to decrease the voltage V_C (negative feedback). By lowering the input impedance Zin_{buffer}, more current will be required to decrease V_C, thus the current I_{C_C} will further increase. The input impedance of the current buffer may be lowered by increasing the transcondutance gm_5:

$$Zin_{buffer} \approx \frac{1}{gm_5} \tag{4.4}$$

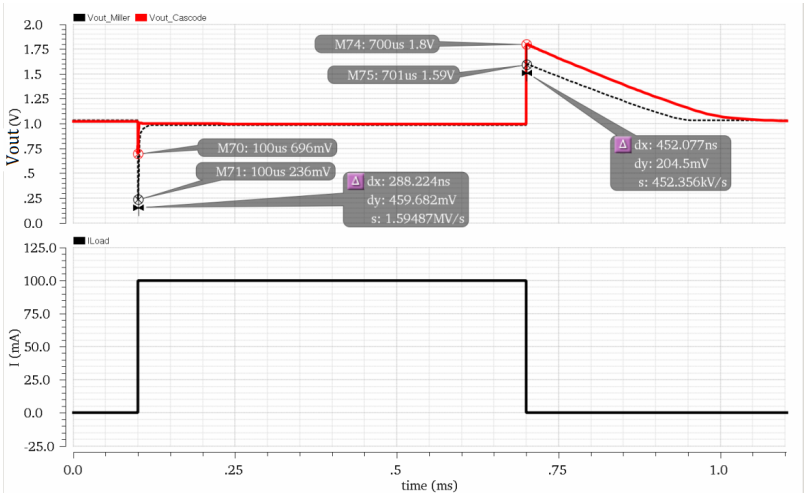


FIGURE 4.6: Dynamic response comparison: Miller (dotted-black) and Cascode (red) compensation.

Conclusively, as seen in Fig. 4.6, cascode compensation yields approximately a 2.5x reduction in undershoot due to the path between the output

and the gate of the pass device V_{pass} created by the compensation capacitor C_C and the current buffer M_5. However, compared to Miller compensation, it gives worse overshoot because of the unidirectional path, which may not provide current to increase V_{pass}.

Fig. 4.7 shows a zoomed-in view of the cascode compensation undershoot transition, the I_{C_C} current, the ratio V_C/V_{pass}, and the load current I_{LOAD}. The figure includes an additional plot (dashed-blue) for comparison, which is the simulation result of adding $500fF$ at the gate of the pass device with the purpose of reducing the time response of the regulator. It can be noted that a few nanoseconds after the start of the load transition, the output voltage stops decreasing (Point A). This is because the high current I_{C_C} lowers the gate of the pass device V_{pass} such that it is able to drive the load current. Then, I_{C_C} will immediately begin to fall down to zero (point B) and consequence $Vout$ will drop (I_{LOAD} still increasing) at a slower rate. During that period, the settling-time will mainly depend on the EA slew-rate current (bias current), since the current across I_{C_C} has been highly reduced due to the slower rate of change of $Vout$. In addition, if the capacitance C_{pass} were higher (dashed-blue), the error amplifier would require more slew-rate current in order to lower the gate of the pass device. As a result, the output voltage could decrease below the "first undershoot" (point A), given higher undershoot. In this particular case, adding $500fF$ at V_{pass}, it decreases approximately $100mV$ after the point A_2.

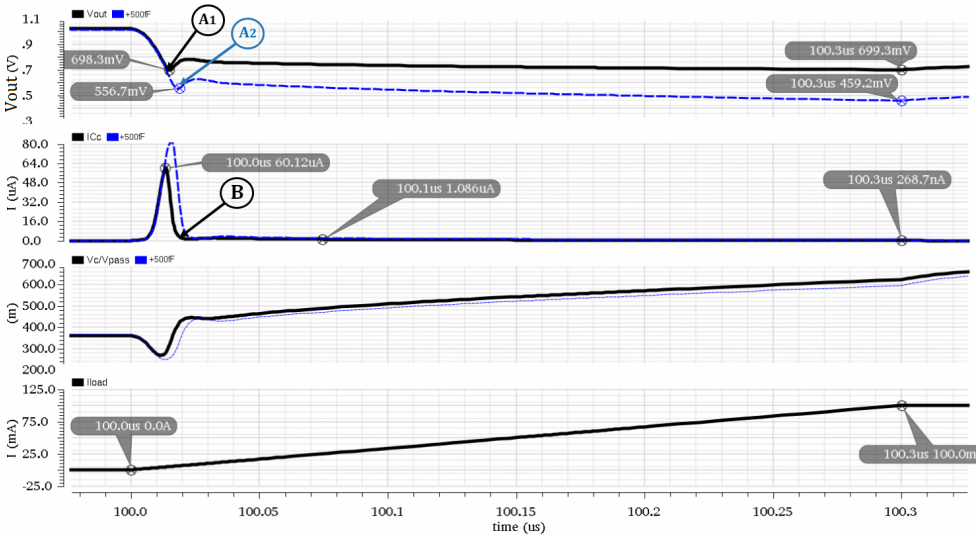


FIGURE 4.7: Undershoot transition, I_{CC}, V_C/V_{pass}, and I_{LOAD}., w/ (dashed-blue) and w/o (black) +500fF at V_{pass}.

Next Fig. 4.8 illustrates the undershoot transition of the previous figure.

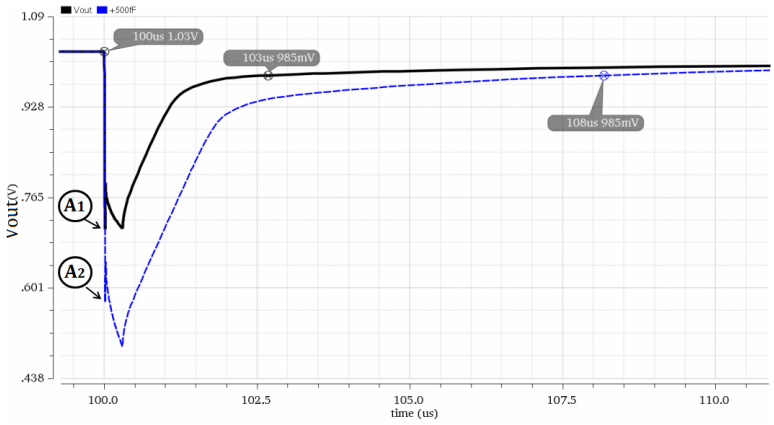


FIGURE 4.8: Zoomed-in view of the undershoot transition w/ (dashed-blue) and w/o (black) +500fF at V_{pass}.

4.2.1 Small-signal AC analysis: Two stage

The cascode compensation small-signal model is shown in Fig. 4.9. Note that it is a simplified model, since it does not include the path that links both V_1 (V_{pass}) and V_{out}. As seen in the schematic in Fig. 4.5, the internal node V_C connects both C_C and gm_1. This path could create a RHP zero [33]; however, its frequency location usually is far away from the GBW, and does not affect the stability response.

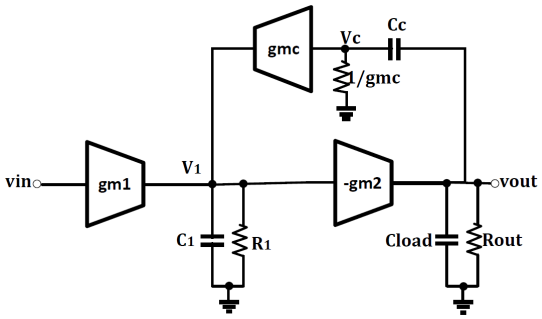


FIGURE 4.9: Two-stage cascode compensation small signal modeling.

$$\begin{cases} v_{in}gm_1 + v_C gm_c = v_1(sC_1 + \frac{1}{R_1}) \\ -v_1 gm_2 + (v_C - v_{out})sC_C = v_{out}(sC_{load} + \frac{1}{R_{out}}) \\ (v_{out} - v_C)sC_C = v_C gm_c \end{cases}$$

Where R_1, R_{out} and $1/gm_c$ are the output resistance of the error amplifier, the equivalent output resistance of the regulator and the input impedance of the current buffer, respectively. gm_c is the transconductance of the transistor M_5, C_1 is the equivalent capacitance at the gate of the pass device (C_{pass}), and C_C is the compensation capacitor.

Solving the three equations system, the transfer function from $Vout$ to Vin can be expressed as follows:

$$\frac{Vout}{Vin} = -\frac{\beta\Delta_{DC}(1+s\frac{C_C}{gm_c})}{(1+\frac{s}{p_1})(1+s\frac{\frac{C_CC_{load}}{gm_c}+C_{load}C_1R_1+C_CC_1R_1}{C_{load}+C_Cgm_2R_1}+s^2\frac{C_{load}C_CC_1R_1}{gm_c(C_{load}+C_Cgm_2R_1)})} \tag{4.5}$$

Where Δ_{DC} is the low frequency gain and β is the feedback factor. They are given as:

$$\Delta_{DC} = gm_1gm_2R_1R_{out} \tag{4.6}$$

$$\beta = \frac{R_{f2}}{R_{f1}+R_{f2}} \tag{4.7}$$

The third order transfer function has three poles and a left half plane zero. They can be expressed as follows:

$$p_1 = -\frac{1}{C_{load}R_{out}+C_Cgm_2R_{out}R_1} \tag{4.8}$$

$$p_2 = -\frac{C_{load}+C_Cgm_2R_1}{\frac{C_CC_{load}}{gm_c}+C_{load}C_1R1+C_CC_1R_1} \tag{4.9}$$

$$p_3 = -\frac{C_{load}C_C+gm_c(C_{load}C_1R_1+C_CC_1R_1)}{C_{load}C_CC_1R_1} \tag{4.10}$$

$$z_1 = -\frac{gm_c}{C_C} \tag{4.11}$$

GBW is the gain-bandwidth which is given as:

$$GBW = \beta p_1\Delta_{DC} = \frac{\beta gm_2gm_1R_1}{C_{load}+C_Cgm_2R_1} \tag{4.12}$$

Furthermore, when the non-dominant poles p_2 and p_3 are close together, they form a conjugate pole pair. Therefore, their location is given as:

$$|p_{2,3}| = -\sqrt{\frac{gm_c(C_{load}+C_Cgm_2R_1)}{C_{load}C_CC_1R_1}} \tag{4.13}$$

and the Quality factor (Q) is given as:

$$Q = \sqrt{\frac{(C_{load}+C_Cgm_2R_1)C_{load}C_CC_1R_1}{gm_c(C_{load}C_1R_1+C_CC_1R_1+C_CC_{load})^2}} \tag{4.14}$$

Cascode compensation is also used in some CL-LDO works [9] [2]. However, the pole equations they are proposing are oversimplified and on occasions, specially in low load current conditions, may not meet the real pole locations.

The simplified equations given by [9] [2] are as follow:

$$p_1 = -\frac{1}{C_Cgm_2R_{out}R_1} \qquad p_2 = -\frac{C_Cgm_2}{C_{load}C_1} \tag{4.15}$$

$$p_3 = -\frac{gm_c}{C_C} \qquad z_1 = -\frac{gm_c}{C_C} \qquad GBW = \frac{\beta gm_1}{C_C} \tag{4.16}$$

$$Q = C_C\sqrt{\frac{gm_2}{C_{load}C_1gm_c}} \qquad |p_{2,3}| = \frac{gm_cgm_2}{C_{load}C_1} \tag{4.17}$$

These equations would match the proposed, as long as the following conditions are met:

$$C_Cgm_2R_1 \gg C_{load} \tag{4.18}$$

$$C_{load} \gg C_C \tag{4.19}$$

$$gm_cC_1R_1 \gg C_C \tag{4.20}$$

4.19 is a typical condition given in two-stage compensated amplifiers [33].

The next study will show a comparison between both analysis (proposed and simplified) under small load current condition. Both calculations and simulation results are given in order to verify the expressions.

Small load current condition stability analysis comparison.

The parameters used for this comparison were extracted from the steady-state simulation of the transistor level circuit:

Parameters	
gm_1	$1.35\mu S$
gm_2	$4.1\mu S$
gm_c	$2.2\mu S$
C_C	$1.5pF$
C_1	$90fF$
C_{load}	$100pF$
R_{out}	$1.7M\Omega$
β	0.5
I_{load}	$150nA$

TABLE 4.1: Two-stage cascode compensation parameters: Small load current condition.

Table 4.2, compares the proposed equations with the simplified equations for different values of R_1. Note that when R_1 gets larger, the difference between both equations decreases. The resistance $R_1 = 250M$ is only used for comparison purpose to see that for very high values of R_1, both expressions give the same result.

At low load current and using a large output capacitor, the simplified equations are no longer valid, unless ensuring high R_1, since gm_2 and gm_c are very small (Conditions 4.18 and 4.20).

Fig. 4.10 shows the simulated stability response. It can be observed that the proposed equations give better accuracy of the pole location compared with the simplified equations.

	$R_{1\,[M\Omega]}$	$p_{1\,[Hz]}$	$\lvert p_{2,3}\rvert$	Q	$z_{1\,[Hz]}$	$GBW_{\,[Hz]}$
Propsed eq.	**5**	716	$329k$	1.4	$233k$	$16.8k$
	10	579	$258k$	1.1	$233k$	$27k$
	25	369	$205k$	0.8	$233k$	$43k$
	250	57	$164k$	0.7	$233k$	$67k$
[9] eq.	**5**	$3k$	$159k$	0.7	$233k$	$71.6k$
	10	$1.5k$	$159k$	0.7	$233k$	$71.6k$
	25	609	$159k$	0.7	$233k$	$71.6k$
	250	60	$159k$	0.7	$233k$	$71.6k$

TABLE 4.2: Comparison table varying R_1; proposed equations, and simplified equations.

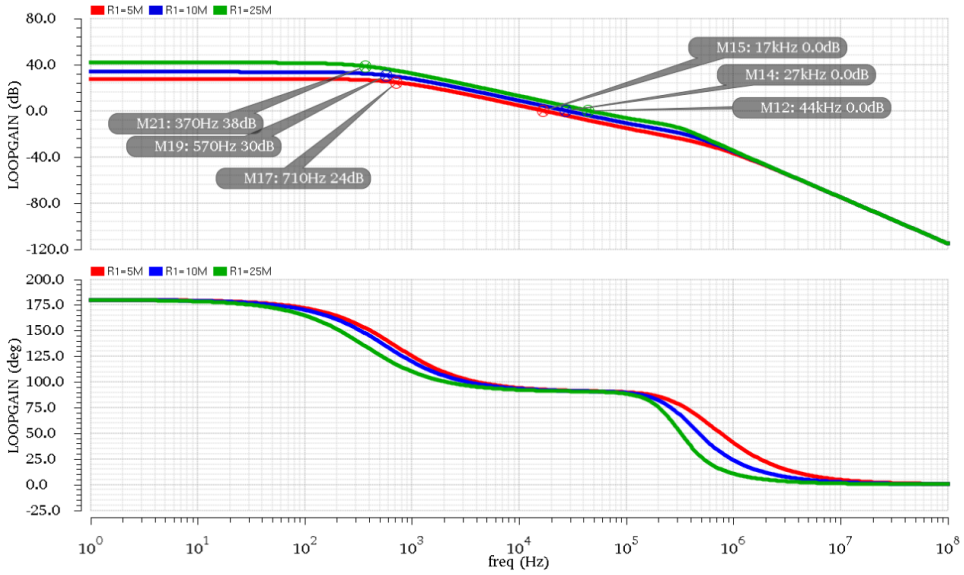


FIGURE 4.10: Stability analysis: $R_1 = 5M$, $R_1 = 10M$, and $R_1 = 25M$.

The same procedure is performed but this time varying C_{load} with the resistance R_1 fixed to $250M\Omega$. The results are given in two tables (4.3, 4.4), since the complex poles become real for high values of C_{load}. Therefore, the frequency location of p_2 and p_3 are given instead.

	C_{load}	$p_{1\,[Hz]}$	$\lvert p_{2,3}\rvert$	Q	$z_{1\,[Hz]}$	$GBW_{\,[Hz]}$
Propsed eq.	**1pF**	61	$1.6M$	2.7	$233k$	$71.6k$
	100pF	57	$164k$	0.7	$233k$	$67k$
[9] eq.	**1pF**	61	$1.6M$	6.8	$233k$	$71.6k$
	100pF	60	$159k$	0.7	$233k$	$71.6k$

TABLE 4.3: Comparison table varying C_{load}; proposed equations, and simplified equations. Q-factor > 0.5.

As seen, both expressions give the same pole location. However, the

Q-factor for $C_{load} = 1pF$ differs greatly between both equations. This is because condition 4.19 is not met.

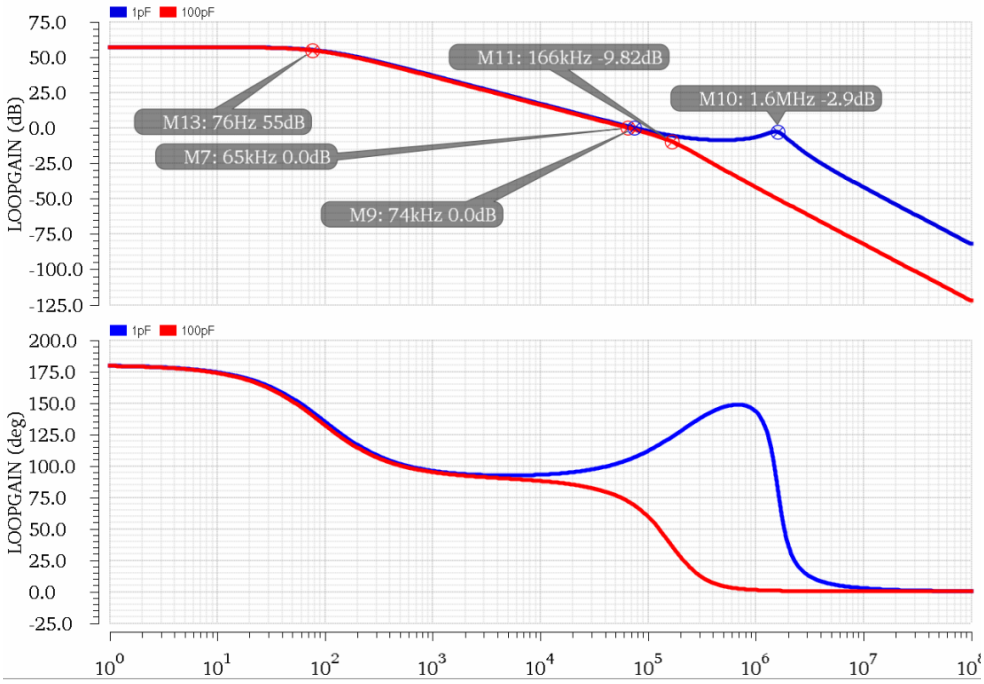


FIGURE 4.11: Low load current stability analysis: $C_{load} = 1pF$ and $C_{load} = 100pF$.

As C_{load} increases, Q-factor decreases. By definition, for $Q < 0.5$, the complex poles split into real poles. Hence, next table is showing the frequencies for p_2 and p_3. It can be observed that for the proposed equations, p_1 and GBW move to lower frequencies as C_{load} increases, since condition 4.18 is not met.

	C_{load}	p_1 [Hz]	p_2 [Hz]	p_3 [Hz]	z_1 [Hz]	GBW [Hz]	Q
Propsed eq.	**500pF**	46	27.9k	233k	233k	54k	0.35
	1nF	37	17.4k	233k	233k	43k	0.27
[9] eq.	**500pF**	61	21.7k	233k	233k	71.6k	0.35
	1nF	61	11k	233k	233k	71.6k	0.21

TABLE 4.4: Comparison table varying C_{load}; proposed equations, and simplified equations. Q-factor < 0.5.

Note that the calculated GBW differs slightly from the simulation shown in Fig. 4.12. This is because p_2 is located before $0dB$ and the GBW expression (4.12) assumes the non-dominant poles are located after $0dB$.

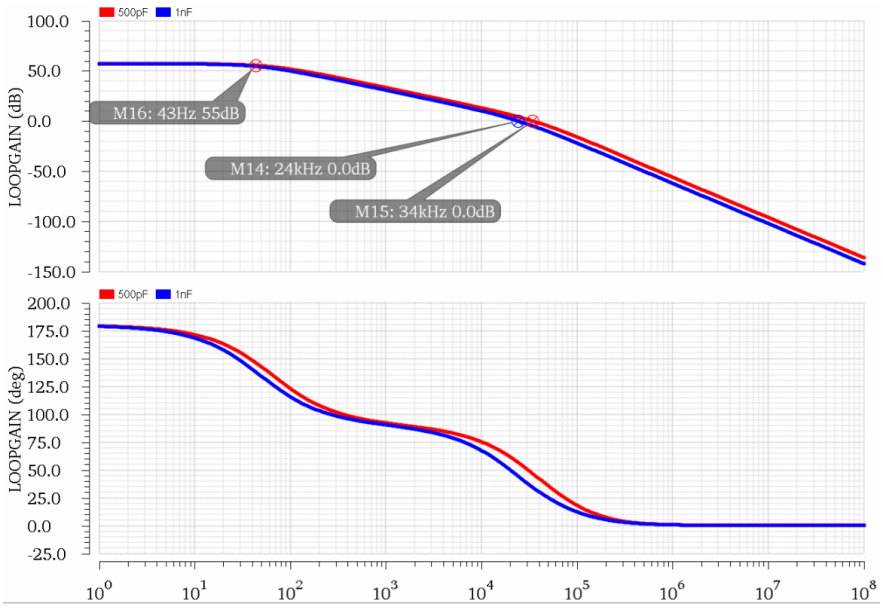


FIGURE 4.12: Low load current stability analysis: $C_{load} = 500pF$ and $C_{load} = 1nF$.

4.3 Adaptive biasing loop (ABL)

The basics of this circuit technique has been already introduced in Chapter 3. In this section the adaptive-biasing loop is analyzed to understand how is affecting the transient response and the stability of the CL-LDO. As seen in next Fig. 4.13, the adaptive biasing loop is formed by transistors M_{abl1}, M_{abl2} and M_{abl3}. The current mirror ratio (1:N) is of the order of 1:500.

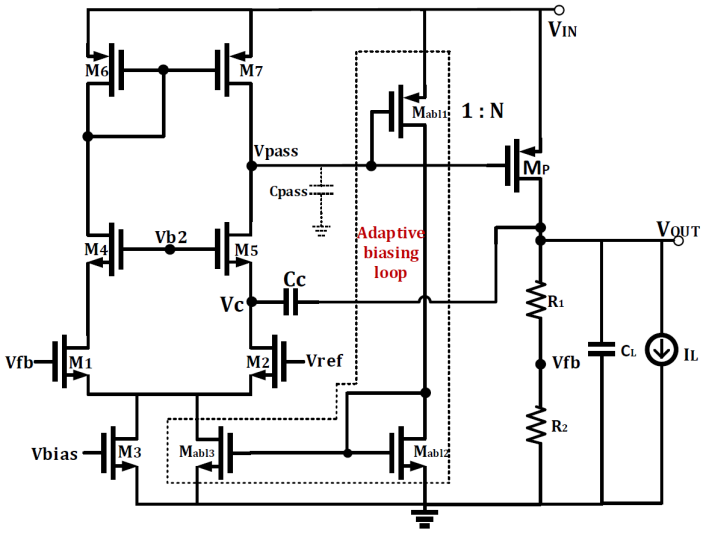


FIGURE 4.13: Schematic view of CL-LDO: Cascode compensation with Adaptive-Biasing Loop.

4.3.1 Dynamic response

Fig. 4.14 presents the dynamic response compared with the previous architectures. The adaptive-biasing loop will be analysed in two cases, with a current-load step from maximum to zero current and vice versa.

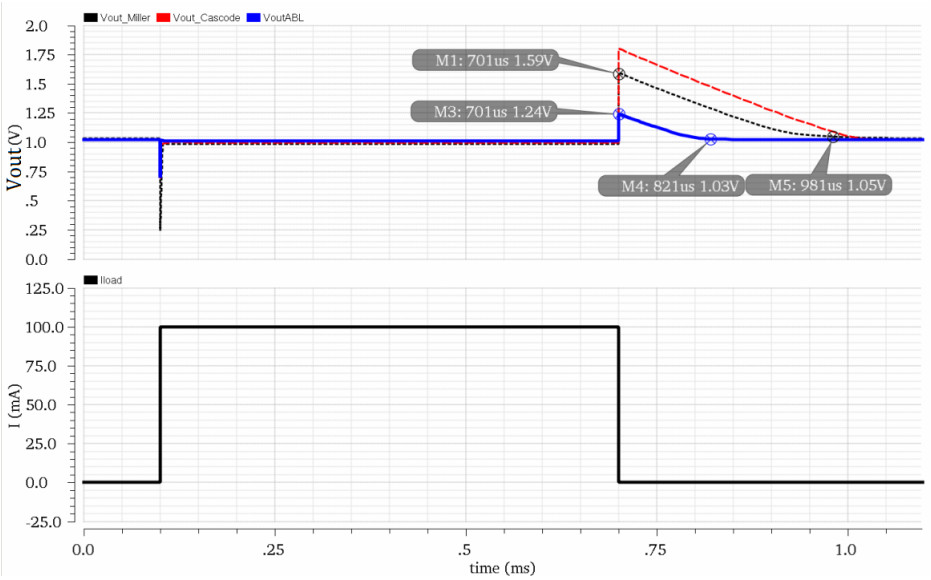


FIGURE 4.14: Dynamic response comparison: Miller (dashed-red), Cascode (dotted-black), Cascode+ABL (blue).

Full-load to no-load current step

At the beginning of the transition, when the load current I_L is high, the ABL is biasing extra current into the error amplifier, increasing the bandwidth and the slew-rate current. Hence, the error amplifier has more capabilities to respond to fast variations of the load current.

The time response of the adaptive biasing loop has to be slow enough to not instantaneously respond to a load current change, otherwise the overshoot would not be improved, because the bandwidth and the slew-rate current of the error amplifier would immediately decrease during the transition. The fact of sensing the current at the gate of the pass device rather directly at the output allows increasing the time response of the adaptive biasing loop, since the current given by the ABL will not start decreasing until the gate of the pass device starts to increase. Hence, when I_L rapidly decreases, the bandwidth and the EA slew-rate current will take longer to decrease (ABL keeps sourcing extra current). As a result of this, the overshoot and the settling-time are highly reduced.

No-load to full-load current step

In this case, at the beginning of the transition (no-load condition), the ABL is not mirroring extra current into the error amplifier, since the load current is zero. Hence, the bandwidth and the slew-rate current of the error amplifier are minimum. However, as mentioned previously, the path between the output and V_{pass} created by the compensation capacitor C_C and

the current buffer M_5 will provide an instantaneous current proportional to the output voltage change:

$$I_{C_C} = C_C \frac{d(V_C - V_{OUT})}{dt} \tag{4.21}$$

Therefore, the gate capacitance will be discharged mainly thanks to the fast path.

In this architecture, the ABL may not contribute to the reduction of the undershoot, since even for an instantaneous current injected into the current bias of the error amplifier at the start of the load transition (during the undershoot transition), the reduction of voltage V_C will attempt to decrease the effective current I_{C_C}, thus balancing the positive effect of the compensation capacitor. However, as can be observed in Fig. 4.15 below, the use of the ABL highly improves the settling-time as well as prevents the decrease of the output after the point A (when I_{C_C} stops injecting current, as previously seen in Fig. 4.7).

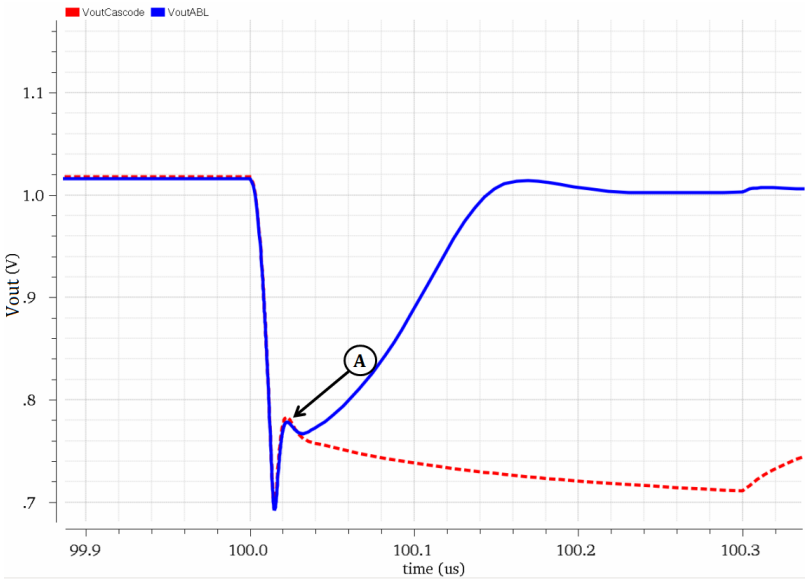


FIGURE 4.15: Zoomed-in view of the undershoot transition: w/ (blue) and w/o (dotted-red) ABL.

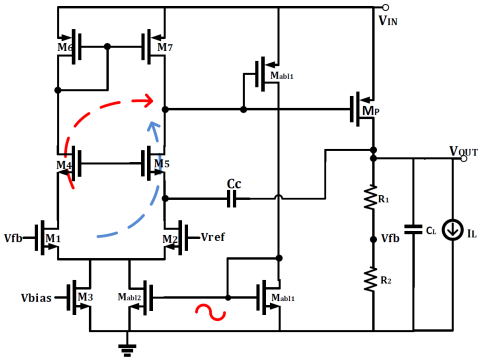
4.3.2 Design considerations

Special attention needs to be made when designing the adaptive biasing loop as it may affect the overall stability of the LDO. The ABL is a positive feedback loop, which can cause sustained oscillations and difficult-to-reverse latched events [28]. It is said that the positive feedback loop is stable if the magnitude of the loop gain is less than 0 dB at all frequencies. Therefore, even when a signal is injected into the loop, the signal fed back is not strong enough. When the positive feedback is stable it does not effect the overall stability of the regulator.

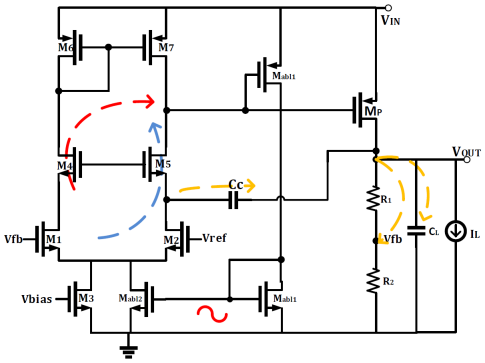
The magnitude of the ABL loop gain would depend on the imbalance of the signal paths. As can be seen in figure 4.16a below, at low-frequencies,

there are two signal paths (red and blue) for the ABL. If transistors are perfectly matched, the LDO output should not be affected by the ABL variations, since they are (ideally) canceled. However, if there is any parasitic pole in the signal transfer paths, the signal could not be canceled at high frequencies. Therefore, the loop gain magnitude could exceeds 0 dB.

The compensation capacitor C_C highly affects the loop gain magnitude of the ABL at high-frequencies, as the signal is splitted through the compensation capacitor C_C (Fig. 4.16b). One way to make sure the regulator keeps stable even when the magnitude of the ABL exceed 0 dB, is by injecting a large signal step into the positive loop and see how the regulator responds. If the LDO regulates the output voltage fast and without any oscillations that means the main-feedback loop (negative feedback) predominate over the positive feedback. Otherwise, the output would oscillate or even would latch to V_{DD}.



(A) Low-frequency path



(B) High frequency path

FIGURE 4.16: Adaptive biasing loop AC signal paths.

Fig. 4.17 shows how the regulator responds to a large current step (0 to $30\mu A$ within 1-ns edge time) injected at V_{pass} under light and full-load conditions with the compensation capacitor fixed to $C_C = 3pF$ in order to verify the positive feedback does not predominates over the negative feedback and causes oscillations and latched events. As can be observed, at full-load condition (blue) the output is regulated back to the target voltage without ringing and good settling-time. During light load condition (dotted-red), the CL-LDO takes longer to regulate the output because there is no extra current biasing the error amplifier, but there are no oscillations. The figure also shows how V_{pass} is moving due to the injected current step.

Conclusively, the positive feedback is not affecting the overall stability of the CL-LDO.

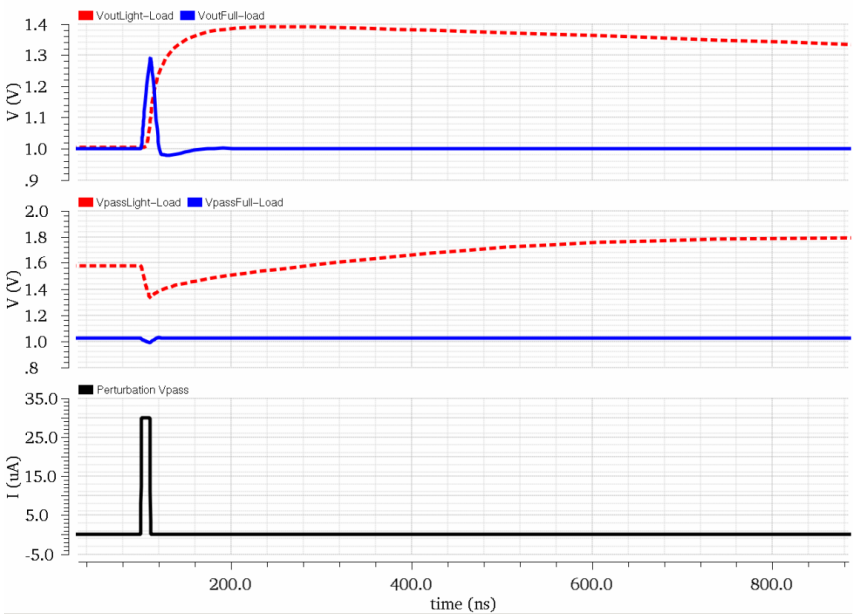


FIGURE 4.17: Step response light (dotted-red) and full-load (blue) conditions.

Next Fig. 4.18 shows the loop gain of the positive feedback for different values of C_C. Note that as the compensation capacitor C_C increases, the loop-gain also increases due to the imbalance of the signal paths which may result in a risk to stability.

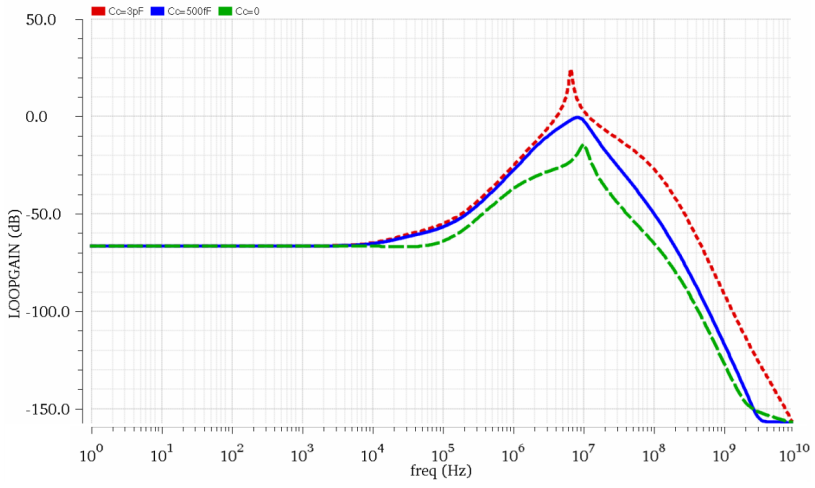
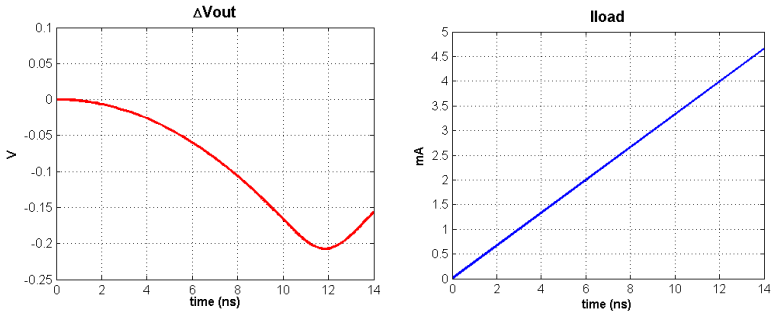


FIGURE 4.18: Adaptive biasing loop gain for $C_C = 0$ (dashed-green), $500fF$ (blue),and $3pF$ (dotted-red).

4.3.3 Effect of pole/zero location on the transient response

In order to examine the movement of the poles and zeros as a function of a load current transition, Cadence was first used to extract the small-signal parameters as a function of time. Then, these parameters were used in Matlab with the pole/zero expressions shown previously in the small-signal analysis of cascode compensation 4.2.1.

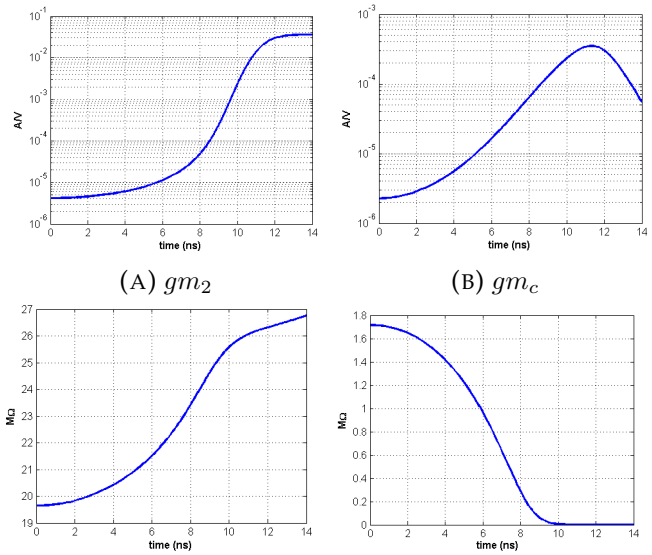
This study was done during the undershoot transition, as seen in Fig. 4.19. The load conditions used in this analysis are the same as commented at the beginning of this Chapter with $C_C = 1.5pF$.



(A) V_{out} (B) I_{load}

FIGURE 4.19: Undershoot curve (a) during the first 14ns of the load current transition (b).

The small-signal parameters extracted from Cadence are as follows:



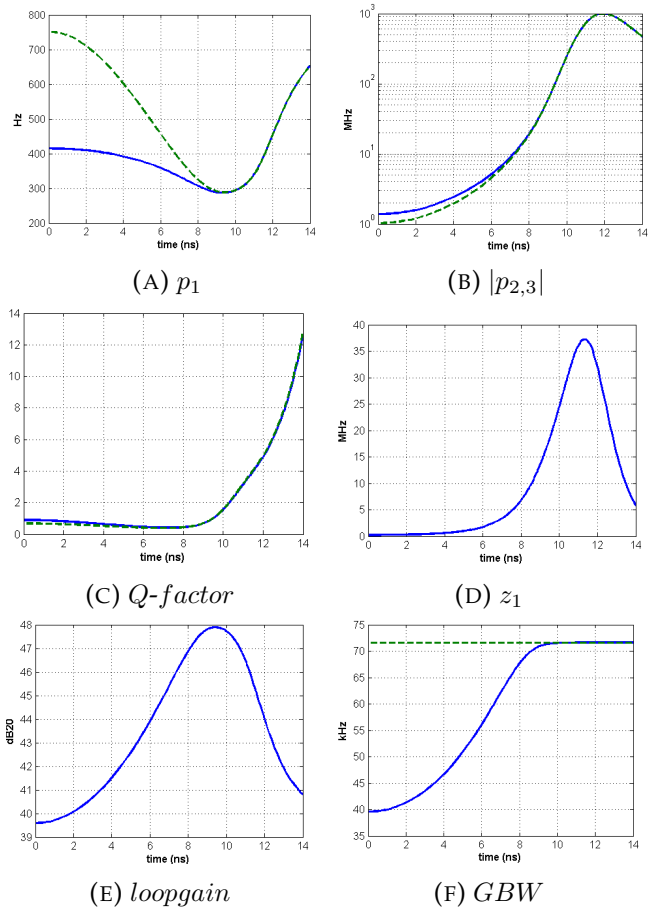
(A) gm_2 (B) gm_c

(C) R_1 (D) R_2

FIGURE 4.20: Small-signal parameters during undershoot curve of Fig. 4.19.

Note that R_2 decreases at a faster rate than gm_2 increases, since R_2 is a function of I_L while gm_2 is a function of $\sqrt{I_L}$. gm_c increases due to the adaptive biasing loop. These parameters were used with the proposed and

simplified expressions given in the small-signal analysis of two-stage cascode compensation in Section 4.4.2 in order to also have a comparison of how vary between them:



(A) p_1 (B) $|p_{2,3}|$

(C) $Q\text{-}factor$ (D) z_1

(E) $loopgain$ (F) GBW

FIGURE 4.21: Pole/zero placement during undershoot transition. Proposed equations (blue), Simplified equations (dotted-green).

The nature of the pole/zero placement is highly dependent on the load current, as illustrated in Fig. 4.21. During the undershoot transition, the conjugate pole pair $|p_{2,3}|$ is moved to higher frequencies, and pole p_1 barely changes. The quality factor Q greatly increases, since gm_2 rises faster than gm_c (equation 4.14). Note that at the beginning of the transition, the proposed equations [4.6-4.13] does not match the simplified equations [4.15-4.17] for p_1 and GBW. This is because gm_2 is such small that does not meet the condition 4.18.

Fig. 4.22 shows the bode at the beginning (green) as well as at the end (blue) of the transition. The high Q-factor at the end of the transition does not degrade the stability of the system, since the complex pole is placed well below 0 dB. The pole/zero behavior is also shown in a Pole-Zero Map (Fig. 4.23). When gm_2 is low, the complex poles have relatively low Q-factor as well as they are located at relatively low frequencies (from 1 to 2). As gm_2 increases, Q-factor and the fundamental frequency increase (from 2 to 3). After the maximum undershoot peak (point 3), the complex poles frequency decreases but Q-factor keep increasing.

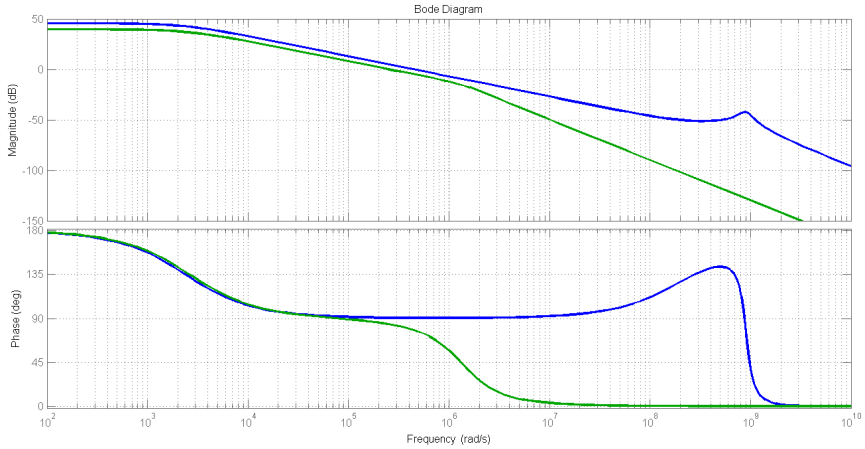


FIGURE 4.22: Bode plot at the beginning of transition (green) and at end of transition (blue).

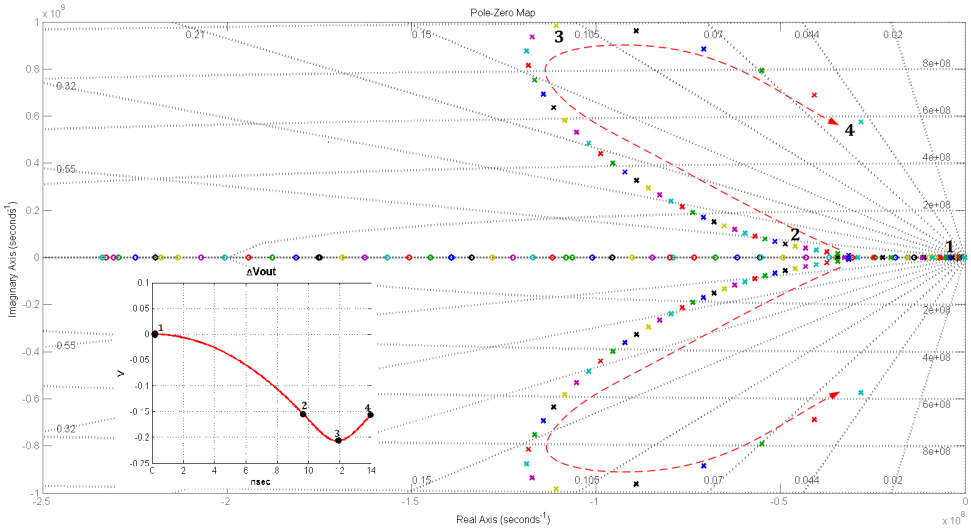


FIGURE 4.23: Pole/Zero Map during undershoot transition.

In conclusion, the stability of the regulator is ensured during the undershoot transition, since the poles are well shifted between them and the large Q-factors occurs only when the conjugate pair is far below 0 dB.

4.4 Adaptive power transistor (APT)

Adaptive power transistor [9] was already introduced in Chapter 3. Next Fig. 4.24 shows the CL-LDO architecture which includes the blocks necessary to implement the techniques described in previous sections:

- Frequency Compensation 1 ⇒ Cascode compensation
- Feedback Network ⇒ Feedback resistors R_1 and R_2
- Error amplifier ⇒ Telescopic amplifier.

- Sub Power transistor M_{P1} pass device
- $I_{bias} \Rightarrow$ Adaptive-Biasing Loop

Besides those, the Adaptive Power Transistor technique requires the addition of an extra stage an power device. In addition, a frequency compensation is proposed to improve the stability response.

- 2n Stage $\Rightarrow$ Non-inverting stage, also works as a current comparator.
- Main power transistor M_{P2} pass device$\Rightarrow$ Much larger (more area) than M_{P1}, since it is designed to drive high load current instead.
- Frequency Compensation 2 $\Rightarrow$ It allows extending the range of load capacitance C_L without degrading the stability. The small-signal analysis and their trade-off are presented later in this section.

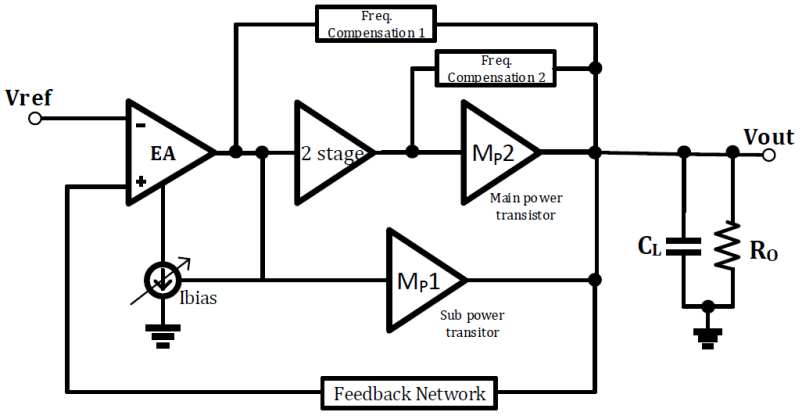


FIGURE 4.24: Structure of the CL-LDO.

Depending on the load current condition, the main power transistor M_{P2} is turned on or off. At light load the regulator is working in two stage mode, both the second stage and main power transistor M_{P2} are turned off and the small sub-power transistor M_{P1} acts as a pass device. Therefore, the architecture can be seen exactly like the previous: two stage cascode compensated with adaptive biasing loop (section 4.3). As load current increases, M_{P2} is turned on by the second stage and starts to deliver I_L to the output, then the regulator transforms into a three stage structure to three stage form. As a result, the gain of the CL-LDO is increased, and therefore the load and line regulation are improved. See equations repeated for convenience below.

$$Load\ regulation = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{OL}}{1 + A_{OL}R_{OL}} \tag{4.22}$$

$$Line\ regulation = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{g_{mp}R_{OL}}{A_{OL}} + \frac{1}{\beta}(\frac{\Delta V_{REF}}{\Delta V_{IN}}) \tag{4.23}$$

Due to the higher transconductance and reduced output resistance arising from the high load current, the pole at the output is moved to high frequencies. thus, ensuring the stability.

Conclusively, moving between two and three stage as a function of the load current allows improving the load and line regulation without stability problems. Furthermore, the area of the sub-power transistor M_{P1} may be much less compared to the main power transistor M_{P2}, since it is designed to drive light load currents instead. Therefore, the equivalent gate capacitance C_{pass1} is greatly reduced, and so the regulator's time response is much less for driving the pass device M_{P1}.

4.4.1 Circuit analysis

In the schematic shown in figure 4.25, the second stage and the main power transistor are formed by $M8 - M13$ and M_{P2}, respectively.

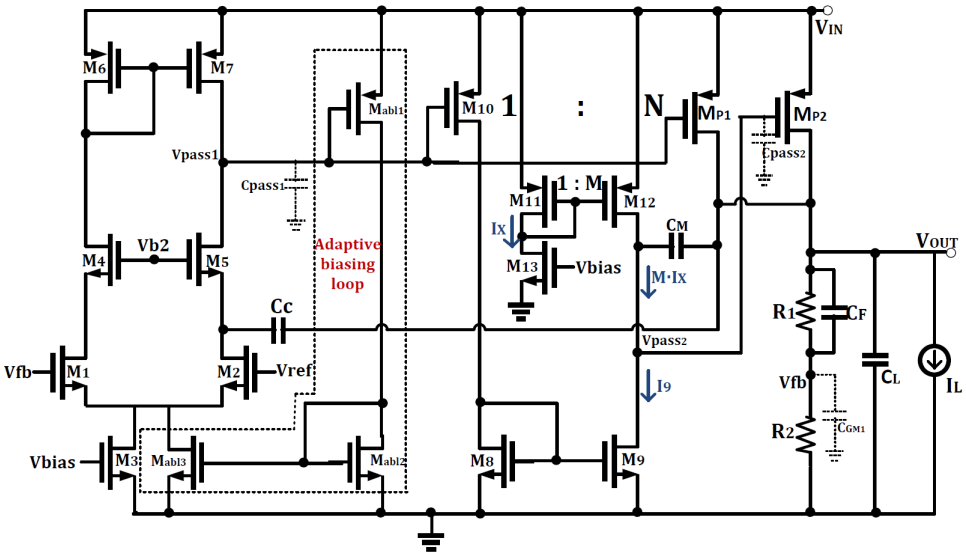


FIGURE 4.25: Schematic view of Adaptive power transistor.

The second stage or current comparator works as follows:
A fraction of load current I_L, which is sensed by M_{10} and then mirrored by M_8 and M_9 is compared with M times the constant current source I_X. As M_{12} is designed to source a current MI_X (threshold current), whenever the current I_9 is lower than MI_X, transistor M_{12} operates in triode region. Therefore, V_{pass2} is approximately equal to V_{IN}, turning the main power transistor M_{P2} off. When the current load I_L increases, and so $I_9 = MI_X$, the transistor M_{12} starts operating in saturation region. Therefore, V_{pass2} decreases, turning the main power transistor on. Note that if the load current further increase, V_{pass2} will proportionally decrease.

Fig. 4.26 is a DC analysis that shows how the output voltage V_{out}, V_{pass1} and V_{pass2} are changing as a function of load current I_L (from 0 to $100mA$). The dotted line indicates the threshold current $\approx 1mA$. As seen, when the load current is smaller than the defined threshold current, the CL-LDO is operating as two-stage ($V_{pass2} = Vin$ and $V_{pass1} \downarrow$). Otherwise, when the load current is higher than the threshold current, it operates in three-stage mode ($V_{pass1} = cst$ and $V_{pass2} \downarrow$) . Fig. 4.27 compares the load transient response with (green) and without (dotted-blue) the adaptive power transistor circuit technique. The adaptive power transistor shows the better dynamic response for the same quiescent current. The undershoot transition

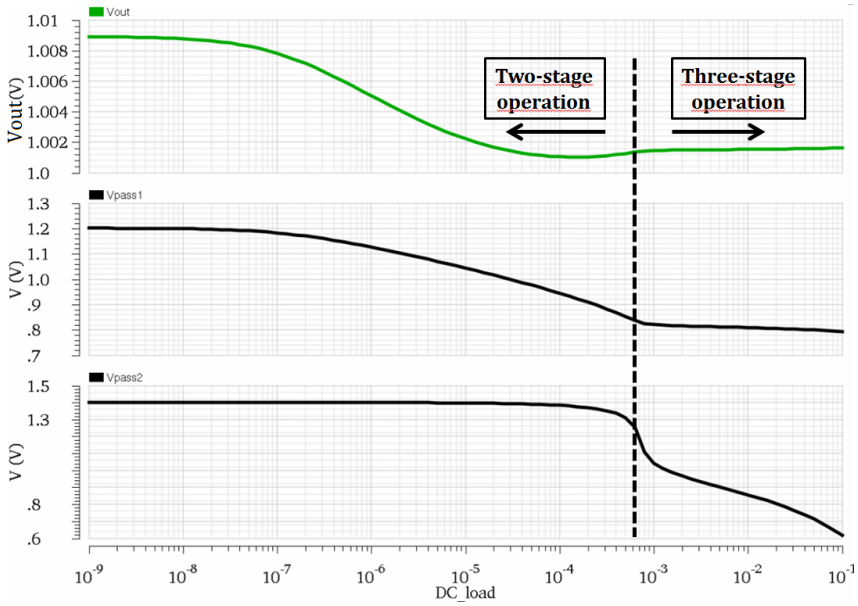


FIGURE 4.26: $Vout$, $Vpass1$, and $Vpass2$ as a function of load current for $Vin = 1.4$.

is improved thanks to the smaller area pass device M_{P1}, i.e., the smaller equivalent gate capacitance C_{pass1} (smaller propagation delay). Therefore, for the same current I_{C_C} the gate of the pass device V_{pass1} will further decrease, giving better magnitude and settling-time. The overshoot transition is also improved thanks to the smaller capacitance C_{pass1} but also by the adaptive biasing loop which in this case the ratio 1:N is set to 1:150 ($\approx 3x$ lower compared to 4.3.) Therefore, for high load conditions the loop bandwidth and slew-rate current is higher (higher bias current), giving better time response during the negative load current step (full load to no load).

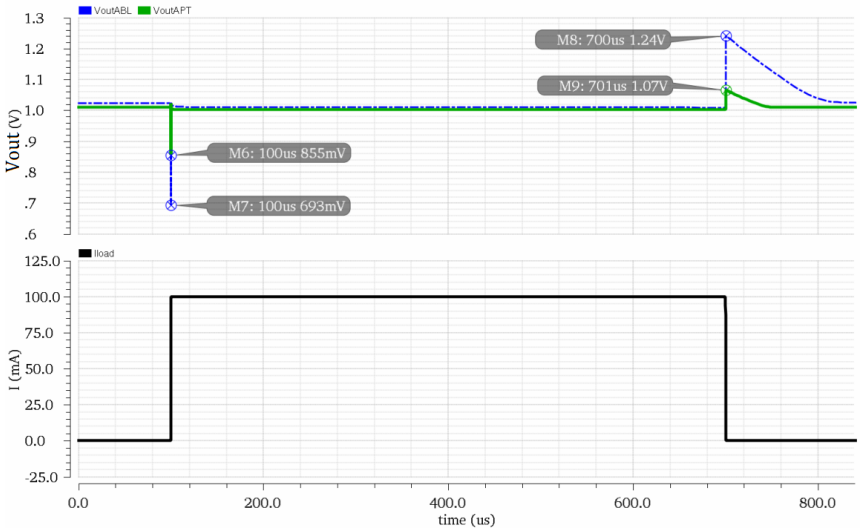


FIGURE 4.27: Dynamic response W/ (green) and W/O (dotted-blue) Adaptive Power Transistor.

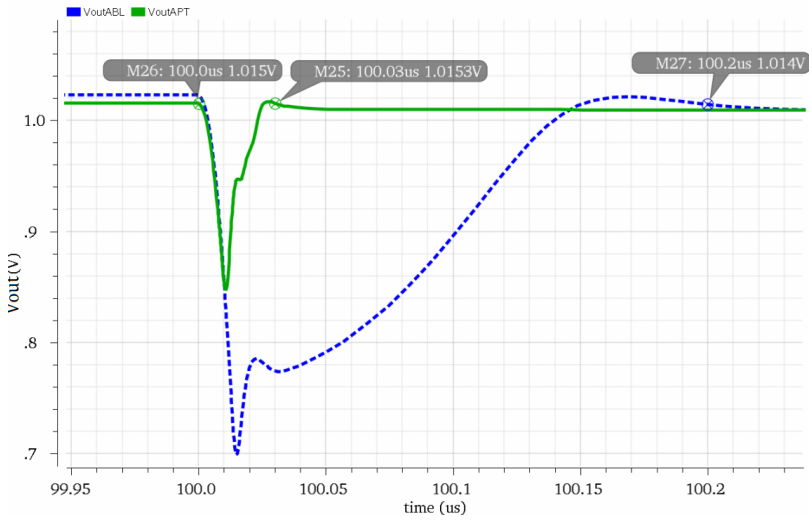


FIGURE 4.28: Zoomed-in view undershoot transition comparison: w/ (green) and w/o (dotted-blue) APT.

The compensation capacitor C_M can cause slewing effects at the gate of M_{P2} that may degrade the overshoot. Next Fig. 4.29 shows the overshoot transition for different values of C_M.

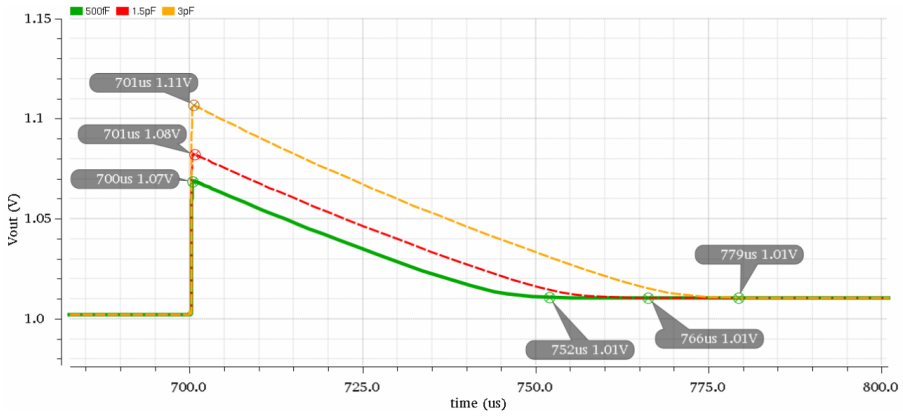


FIGURE 4.29: Overshoot transition for $C_M = 500fF$ (green), $C_M = 1.5pF$ (dotted-red) and $C_M = 3pF$ (dashed-orange).

The architecture also includes a capacitor C_F in the feedback-resistive network to improve the stability of the CL-LDO [20]. The parasitic capacitance $C_{G_{M1}}$ represents the capacitance seen at the gate of the input transistor M_1 which basically consists of the gate-drain capacitance C_{gd} multiplied by the gain across M_1 (Miller effect). As $R_1 \| R_2$ is moderately high in order to reduce quiescent current, the feedback pole p_F may reside before f_{0dB}, and therefore negatively affect the stability of the system.

The capacitor C_F creates a left half plane (LHP) zero at medium frequencies. This can be shown by taking the transfer function from Fig. 4.30 which is given by:

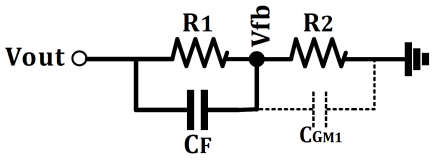


FIGURE 4.30: Feedback-resistive network.

$$\frac{Vfb}{Vout} = \frac{R_2}{R_1 + R_2} \frac{1 + sC_F R_1}{1 + s(C_F + C_{G_{M1}})R_1 \| R_2} \tag{4.24}$$

Therefore, the zero z_F is created which is given by:

$$z_F = -\frac{1}{C_F R_1} \tag{4.25}$$

Furthermore, the feedback pole is moved to lower frequencies.

$$p_F = -\frac{1}{(C_F + C_{G_{M1}})R_1 \| R_2} \tag{4.26}$$

As the frequency of the LHP zero (z_F) is near to the non-dominant feedbackpole p_F, it cancels its effect, and therefore the frequency response is improved.

4.4.2 Small-signal AC analysis: Three stage

Due to the architecture transformation, the stability of the three stage CL-LDO is also analysed. The addition of capacitor C_M forms a Nested Miller Compensation topology [33] [19] which is an extension of the Miller compensation used in two-stage.

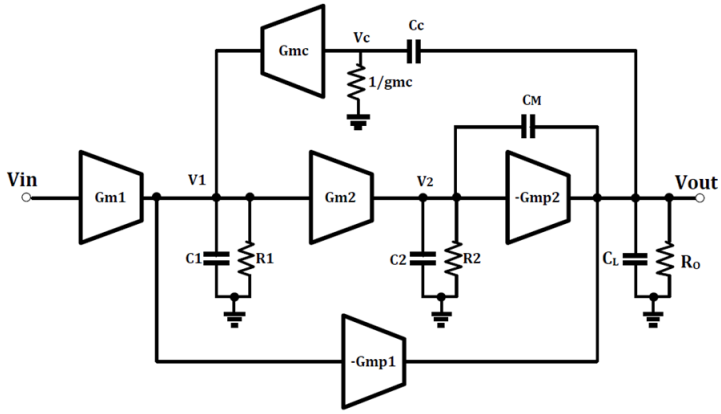


FIGURE 4.31: Three-stage APT small-signal modeling.

$$\begin{cases} v_{in}gm_1 + v_c gm_c = v_1(sC_1 + \frac{1}{R_1}) \\ v_1 gm_2 = v_2(sC_2 + \frac{1}{R_2}) + (v_2 - v_{out})sC_M \\ -gmp_2 v_2 + (v_2 - vout)sC_M - gmp_1 v_1 = v_{out}(sC_L + \frac{1}{R_O}) + (v_{out} - v_c)sC_C \\ (v_{out} - v_c)sC_C = gm_c v_c \end{cases}$$

Solving the four equations system, the transfer function from v_{out} to v_{in} can be expressed as follows:

$$\frac{vout}{vin} = -\frac{\beta\Delta_{DC}(1 + s\frac{C_C}{gm_c})(1 - s\frac{C_M}{gmp_2})(1 + s\frac{gmp_1 C_M}{gm_c gm_2})}{(1 + \frac{s}{p_1})(1 + s\frac{(R_1 gmp_1 + \frac{gmp_2}{gm_c})C_M}{gmp_2 gm_2 R_1} + s^2\frac{(R_1 gmp_1 + \frac{gmp_2}{gm_c})C_1 C_M}{gm_2(gm_c gmp_1 R_1 + gmp_2)}(1 + \frac{s}{p_4})} \tag{4.27}$$

Where Δ_{DC} is the low frequency gain and β is the feedback factor. They are given as:

$$\Delta_{DC} = gm_1 gm_2 gmp_2 R_1 R_2 R_O \tag{4.28}$$

$$\beta = \frac{R_{f2}}{R_{f1} + R_{f2}} \tag{4.29}$$

The four order transfer function has four poles, two left half plane zero and one right plane zeros. They can be expressed as follows:

$$p_1 = -\frac{1}{C_C gm_2 gmp_2 R_1 R_2 R_O} \tag{4.30}$$

$$p_2 = -\frac{gmp_2 gm_2 R_1}{(R_1 gmp_1 + \frac{gmp_2}{gm_c})C_M} \tag{4.31}$$

$$p_3 = -\frac{gm_c gmp_1 R_1 + gmp_2}{gmp_2 R_1 C_1} \tag{4.32}$$

$$p_4 = -\frac{gmp_2}{C_2 + C_L} \tag{4.33}$$

$$z_{LHP_1} = -\frac{gm_c}{C_C} \tag{4.34}$$

$$z_{LHP_2} = -\frac{gmp_2}{C_M} \tag{4.35}$$

$$z_{RHP} = \frac{gm_c gm_2}{gmp_1 C_M} \tag{4.36}$$

GBW is the gain-bandwidth which is given as:

$$GBW = \beta p_1 \Delta_{DC} = \frac{\beta gm_1}{C_C} \tag{4.37}$$

Furthermore, when the non-dominant poles p_2 and p_3 are close together, they form a conjugate pole pair. Therefore, their location is given as:

$$|p_{2,3}| = -\sqrt{\frac{gm_2(gm_c gmp_1 R_1 + gmp_2)}{(R_1 gmp_1 + \frac{gmp_2}{gm_c})C_1 C_M}} \tag{4.38}$$

and the Quality factor (Q) is given as:

$$Q = \sqrt{\frac{gm_2 C_1 gmp_2^2 R_1^2}{(R_1 gmp_1 + \frac{gmp_2}{gm_c}) C_M (gm_c gmp_1 R_1 + gmp_2)}} \tag{4.39}$$

To validate the given expressions, the stability of the small-signal model was simulated. The parameters used were extracted from a simulation of the circuit under maximum load current condition $I_L = 100mA$ which are given below in table 4.5.

Parameters	
gm_1	$200\mu S$
gm_2	$150\mu S$
gm_c	$400\mu S$
gmp_1	$15mS$
gmp_2	$500mS$
C_1	$90fF$
C_2	$20fF$
C_c	$3pF$
C_L	$100pF$
R_1	$200k\Omega$
R_2	$200k\Omega$
R_0	12Ω
β	0.5
I_L	$100mA$

TABLE 4.5: Three-stage CL-LDO parameters (full-load).

Next table 4.6 gives the results for several values of C_M using the previous expresions. Fig. 4.32 shows the simulated results for comparison.

$\boldsymbol{C_M}$	$\boldsymbol{p_{1}}_{[Hz]}$	$\boldsymbol{\lvert p_{2,3}\rvert}_{[Hz]}$	$\boldsymbol{Q}$	$\boldsymbol{p_{4}}_{[Hz]}$	$\boldsymbol{z_{1_{LHP}}}_{[Hz]}$	$\boldsymbol{z_{2_{LHP}}}_{[Hz]}$	$\boldsymbol{z_{1_{RHP}}}_{[Hz]}$	$\boldsymbol{GBW}_{[Hz]}$
$\boldsymbol{500fF}$	$1.47k$	$184M$	6	$796M$	$21.2M$	$159G$	$62.8G$	$5.31M$
$\boldsymbol{2pF}$	$1.47k$	$92M$	3	$796M$	$21.2M$	$29.8G$	$15.7G$	$5.31M$
$\boldsymbol{5pF}$	$1.47k$	$58M$	2	$796M$	$21.2M$	$15.9G$	$6.28G$	$5.31M$

TABLE 4.6: pole/zero location varying C_M.

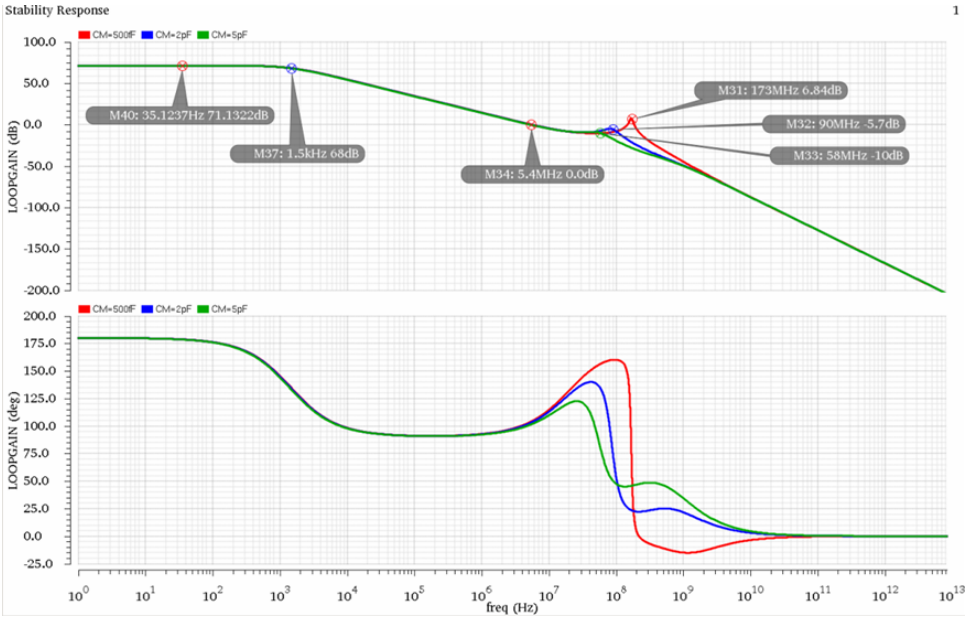


FIGURE 4.32: Three-stage model stability analysis.

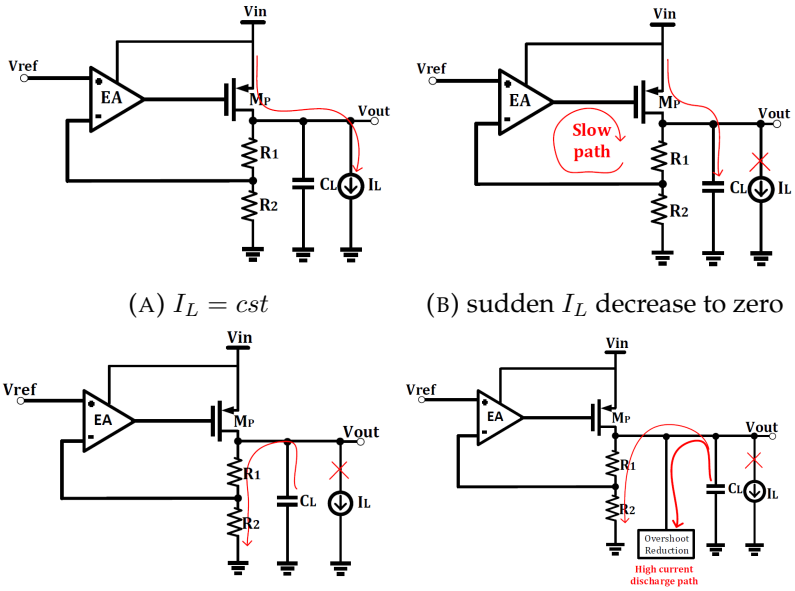
The capacitor C_M has a strong influence on the Q-factor of the non-dominant complex poles. Thus, an increase in C_M will reduce Q significantly, while slightly reducing the ω_0 ($|p_{2,3}|$). Therefore, the addition of C_M have a trade-off between the location of the complex poles and a flat response. Furthermore, the output pole p_4 is pushed to higher frequencies due to pole-splitting effect. Consequently, compensating the CL-LDO with larger C_L may be easier using compensation capacitor C_M.

4.5 Overshoot reduction network

The explanation provided earlier in 2.3.4.2 is repeated here for convenience. After the maximum overshoot peak, V_{OUT} takes a long time to recover the regulated voltage ($1V$). This is mainly because when fast negative load current step occurs (full load to 0), the regulator takes some time to react, and meanwhile the pass device keeps sourcing current which charges the output capacitor C_L (figure 4.33b). Once the regulator responds, the pass device stop sourcing current. However, as the output capacitor is charged due to the slowness of the regulator, the output voltage may not return back to its targeted voltage until it does not fully discharge (figure 4.33c). As a consequence, the settling time would depend on the sinking capabilities the regulator has in order to discharge and slew the output capacitor. In this particular case, the only path to discharge the capacitor is through the feedback network, which for quiescent current reasons, only sinks $50nA$.

The overshoot reduction network is formed by transistor M_p, capacitor Cp, and resistor Rp (Fig. 4.34). When the current load suddenly decreases, capacitor Cp senses the change in voltage at V_{pass2} and it then couples to the gate of M_p. Therefore, it provides a high current path to quickly discharge the output capacitor C_L (4.33d).

It can be seen in next Fig. 4.35 that the addition of the overshoot reduction network yields approximately a 17x reduction in the settling-time.



(A) $I_L = cst$ (B) sudden I_L decrease to zero

(C) capacitor discharging only through feedback network path (D) capacitor discharging trough high current path

FIGURE 4.33: Overshoot transition.

The figure also includes the current I_{MP} generated by the overshoot reduction network. Note that in steady-state, the current flowing through M_P is around $100nA$.

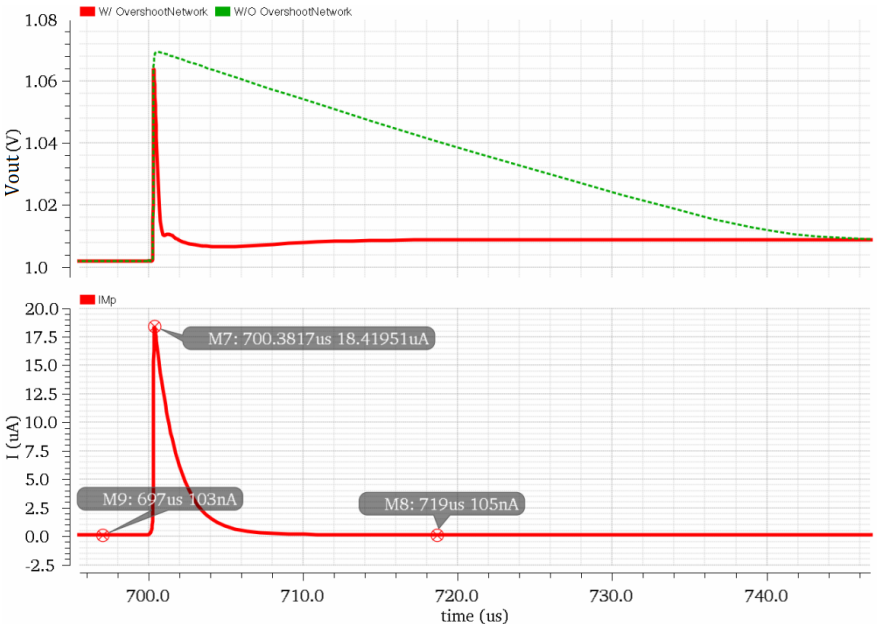


FIGURE 4.35: Overshoot transition w/ (orange) and w/o (dotted-green) overshoot reduction network.

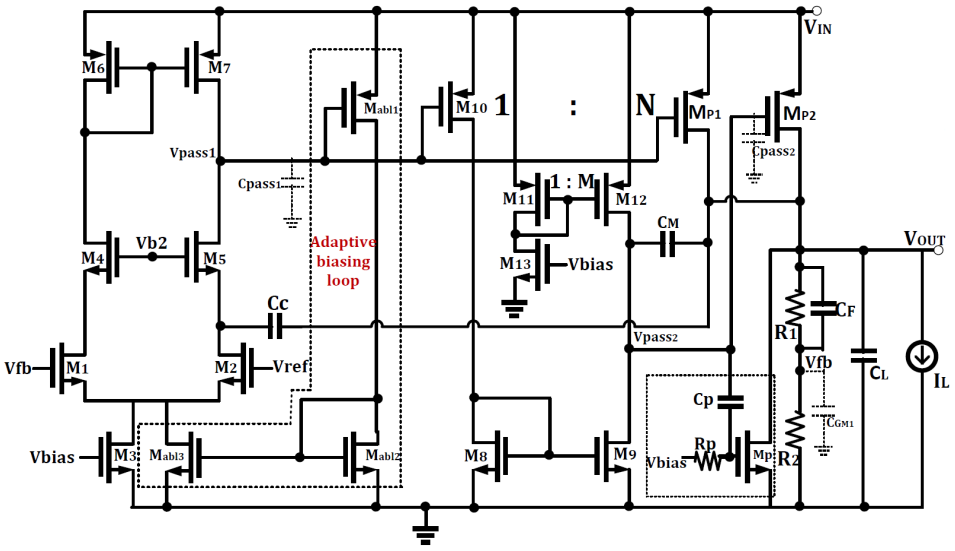


FIGURE 4.34: Schematic view of Adaptive power transistor + overshoot reduction network.

4.6 Proposed Gm-Boost

As mentioned previously in 4.2, lowering the input impedance of the current buffer (transistor M_5), the effective slew-rate current may be greatly increased, allowing better dynamic performance.

$$Zin_{buffer} \approx \frac{1}{gm_c} \tag{4.40}$$

It is well known that the transconductance can be increased either by increasing the biasing current of the transistor or by increasing the size. Both approaches would result in quiescent current and parasitic capacitance C_{pass1} increase. The gm-boost proposed in this section allows to substantially enhance the M_5 transconductance without hardly increase the quiescent current.

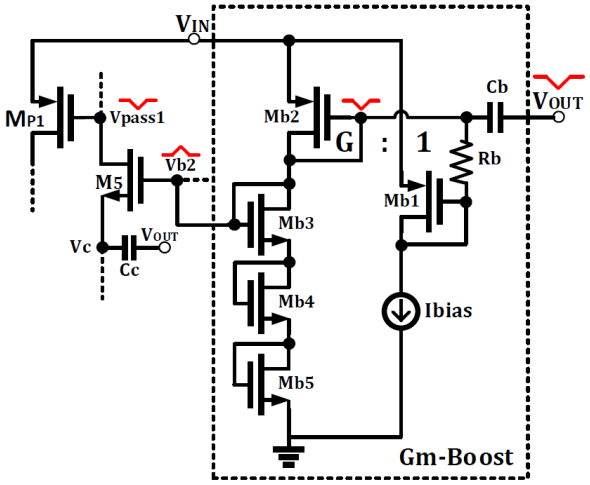


FIGURE 4.36: Gm-Boost operation.

The circuit that implements this technique is shown in 4.36. The gm-boost dynamically sets the bias voltage of transistors M_4 and M_5 by means of transistors Mb_1-Mb_5, the resistor Rb and the coupling capacitor Cb. The principle of operation is also illustrated in Fig. 4.36. When the output suddenly decreases, the change is sensed by Cb and is then coupled to the gate of transistor Mb_2. Then, transistor Mb_2 will source more current, causing an increase of the voltage V_{b2} proportional to the output voltage rate of change, and therefore, as explained in the following of this section, lowering the gate of the pass device M_{P1}.

Commonly, the gm-boost is connected between the source (V_C) and the gate (V_{b2}) of cascode transistor M_5 [16]. However, the capacitor C_C would be used to sense the output voltage changes instead, and therefore the DC bias of the gm-boost transistor would be forced to operate at V_C. Consequently, the dimension and the bias current required may be relatively large, affecting the efficiency and the loop response time of the gm-boost (discussed below in design considerations 4.6.1). Connecting the gm-boost between $Vout$ and V_{b2} allows independent DC bias, and therefore smaller transistors and quiescent current. The only disadvantage is that it requires an extra capacitor C_b for sensing the output voltage changes.

The dynamic response with and without the gm-boost is presented in Fig. 4.37. As seen, the undershoot is improved $64mV$ (44%) and the overshoot is not affected because of the current buffer that makes the path unidirectional.

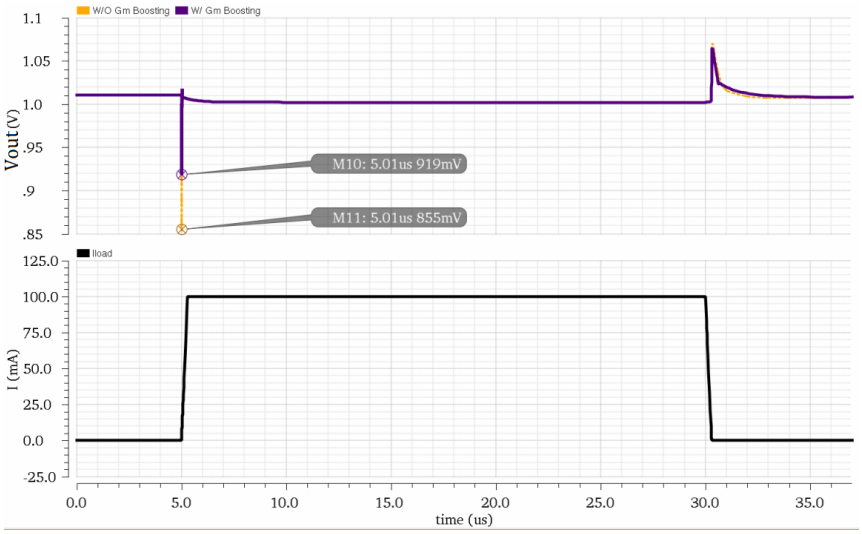


FIGURE 4.37: Dynamic response W/ (purple) and W/O (dotted-orange) gm-boost.

The increase in V_{b2} will attempt to increase the source of M_5 (V_C) when this should decrease (negative feedback). Therefore, the compensation capacitor will generate more current (($V_C - V_{out}$)↑). This increase in current will rise the transconductance of M_5, see Fig. 4.38.

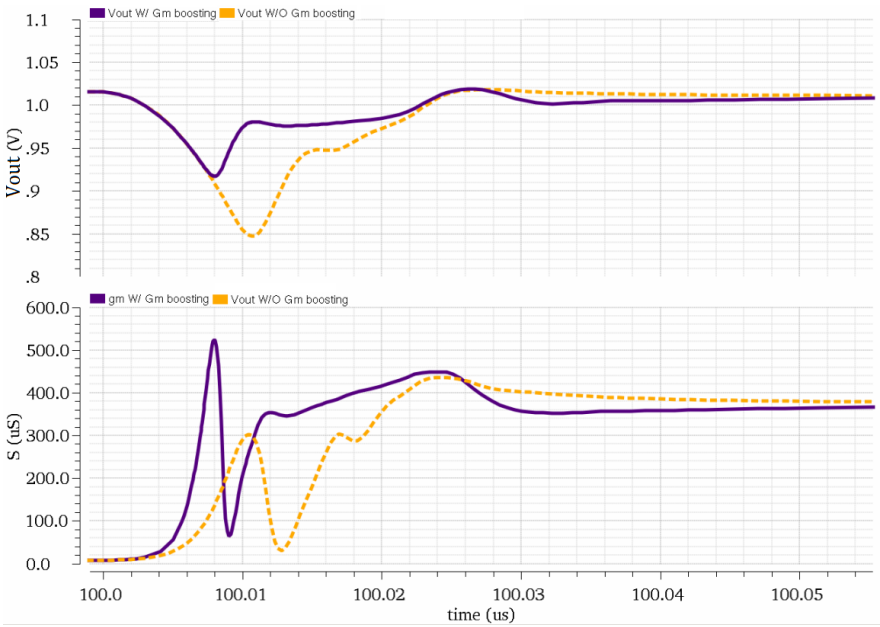


FIGURE 4.38: Undershoot transition and transconductance gm_5 w/ (purple) and w/o (dotted-orange) gm-boost.

The following Fig. 4.39 shows for both cases (w/ and w/o gm-boost) the current I_{CC}, the voltage Vgs of transistor M_5, and the voltage V_C, respectively. Note how I_{C_C} rapidly increases when the gm-boost is used. This is because more current is required to lower the voltage V_C, due to the increase in V_{b2}. It can also be observed that at steady-sate the gm-boost acts as a DC bias circuit (same V_{gs} for both). Hence, the addition of the gm-boost does not requires much more current than a common DC bias circuit.

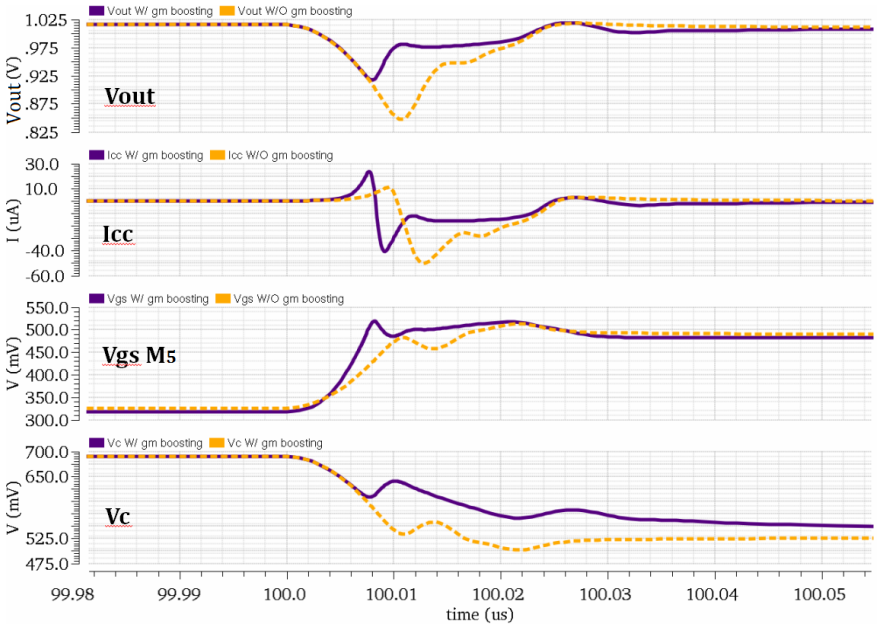


FIGURE 4.39: Undershoot transition w/ (purple) and w/o (dotted-orange) gm-boost.

4.6.1 Design considerations

The gm-boost has to be designed with enough magnitude (gain) and bandwidth to sufficiently increase the bias voltage V_{b2} and to quickly respond fast output voltage variations, respectively. However, there is trade-off between gm-boost performance and stability of the system.

Next Fig. 4.40 presents the CL-LDO stability analysis with and without the gm-boost at high load condition ($10mA$). Note that when the gm-boost is used, the loop gain of the main feedback loop (dashed-red) follows the gm-boost loop gain (dotted-yellow). Consequently, the phase margin is degraded 27° compared without gm-boost (blue).

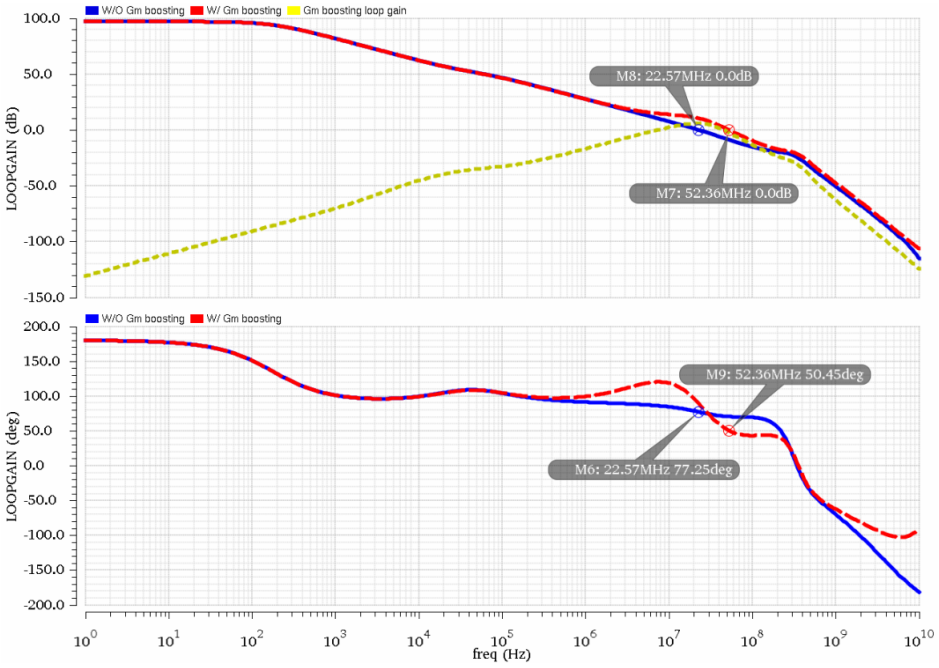


FIGURE 4.40: Stability analysis w/ (dashed-red) and w/o (blue) gm-boost loop (dotted-yellow) at $10mA$ load current condition.

Phase margin as function of gm-boost loop gain is illustrated in Fig. 4.41. As the gain increases (by increasing the mirror ratio G:1), the phase margin of the main feedback loop decreases. The loop gain and phase of the gm-boost for different gain magnitude are also depicted in Fig. 4.42.

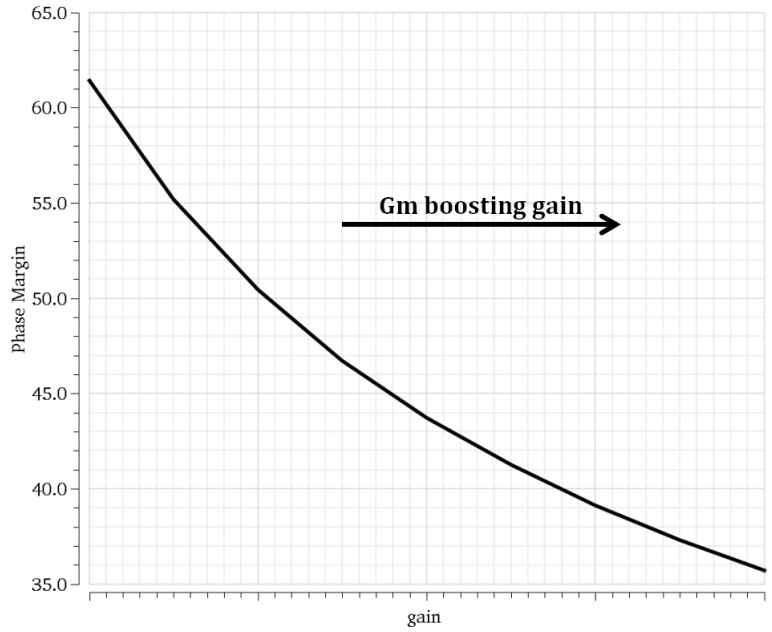


FIGURE 4.41: CL-LDO phase margin as function of gm-boost loop gain at $10mA$ load current condition.

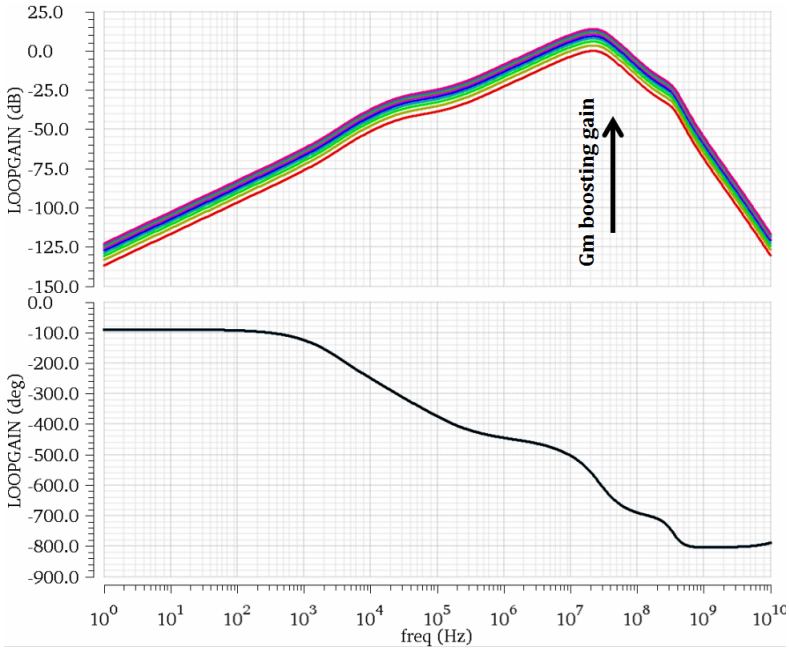


FIGURE 4.42: Gm boosting loop for different loop gain.

Fig. 4.43 shows how the gm-boost varies as a function of load current. The loop is mainly affected by the output pole (V_{out}) and the transconductance gm_5 which varies due to the adaptive biasing loop.

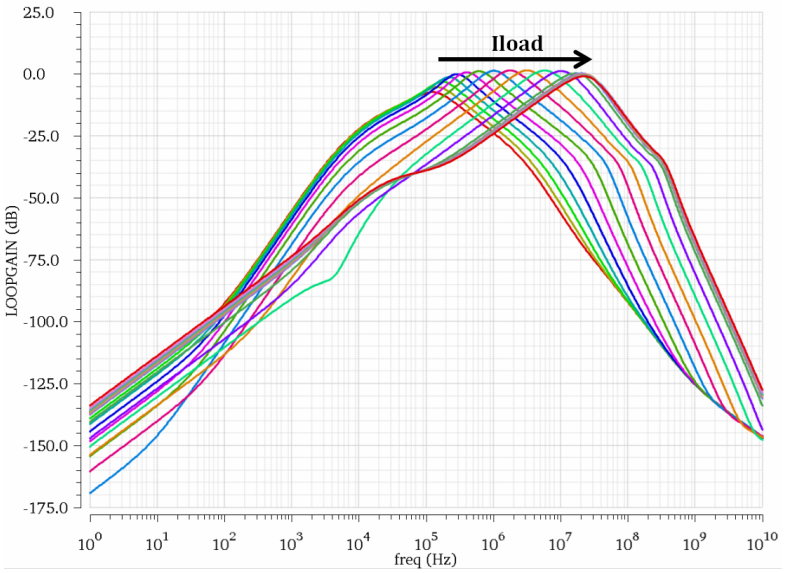


FIGURE 4.43: Gm-boost loop as a function of load current at $10mA$ load current condition.

Furthermore, the gm-boost loop highly affects the PSR, specially at light load current conditions. This will be shown in more detail in the next following Chapter 5. In addition, the parasitic capacitance at the output node of the gm-boost V_{b2} determines how fast is the loop, i.e., the bandwidth. Therefore, special care should be taken when sizing transistors Mb_3, M_4 and M_5, since the larger the area, the larger the parasitic capacitance would be. The parasitic capacitance may affect the bandwidth of the gm-boost loop in such a way that the loop may be too slow to respond and so give any improvement. Next Fig.4.44 below shows how the gm-boost performance is affected by adding different values of parasitic capacitance at V_{b2}. Observe that even small values of parasitic capacitance, directly affects the dynamic performance.

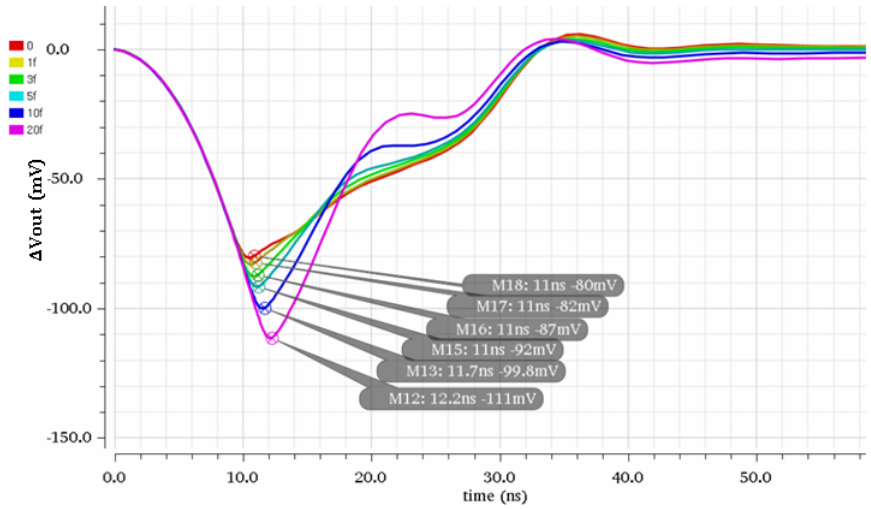


FIGURE 4.44: Impact of parasitics on Gm-Boost performance.

Parasitic cap.	**Undershoot**
$+\mathbf{1}\boldsymbol{fF}$	$+2.5\%$
$+\mathbf{3}\boldsymbol{fF}$	$+8.75\%$
$+\mathbf{5}\boldsymbol{fF}$	$+15\%$
$+\mathbf{10}\boldsymbol{fF}$	$+19.8\%$
$+\mathbf{20}\boldsymbol{fF}$	$+38.8\%$

TABLE 4.7: Undershoot increment as function of parasitic capacitance in the gm-boost output node V_{b2}.

Chapter 5

Complete CL-LDO Circuit Design and Performance Characterization

The addition of the different techniques presented in Chapter 4 allowed to reduced the undershoot/overshoot problems down to acceptable levels. This chapter presents the final design of the proposed CL-LDO and its complete characterization. All simulations have been realized with Cadence and TSMC $40nm$ Low Power (LP) CMOS technology. The conditions of each simulation and their considerations are also given.

The required specifications for the CL-LDO are repeated in table 5.1 for convenience.

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{IN}	1.33	1.4	1.47	V
Output voltage	V_{OUT}	-	1	-	V
Drop-out voltage	V_{DO}	-	400	-	mV
Quiescent current	I_Q	-	900	-	nA
Load current	I_L	0	-	100	mA
Edge time	$t_{rise/fall}$	0	300	-	ns
Current pulse width	$I_{L_{width}}$	–	20	–	μs
Output capacitor	C_L	-	100	500	pF
Load transient regulation	$\Delta V_{OUT} + \Delta V_{OS}$	-7	-	$+7$	%
Phase margin	PM	45	-	-	$^\circ$
Gain margin	GM	10	-	-	dB

TABLE 5.1: Performance Characteristics of the CL-LDO.

5.1 Final CL-LDO design

The final design is illustrated in Fig. 5.1 bellow. Instead of feedback resistors R_1 and R_2 (Fig. 4.34), the feedback-network is realized by a string of four diode-connected pMOS transistors biased in the subthreshold region to minimize quiescent current as well as silicon area. The size of the key transistors and the most relevant parameters are demonstrated in table 5.2.

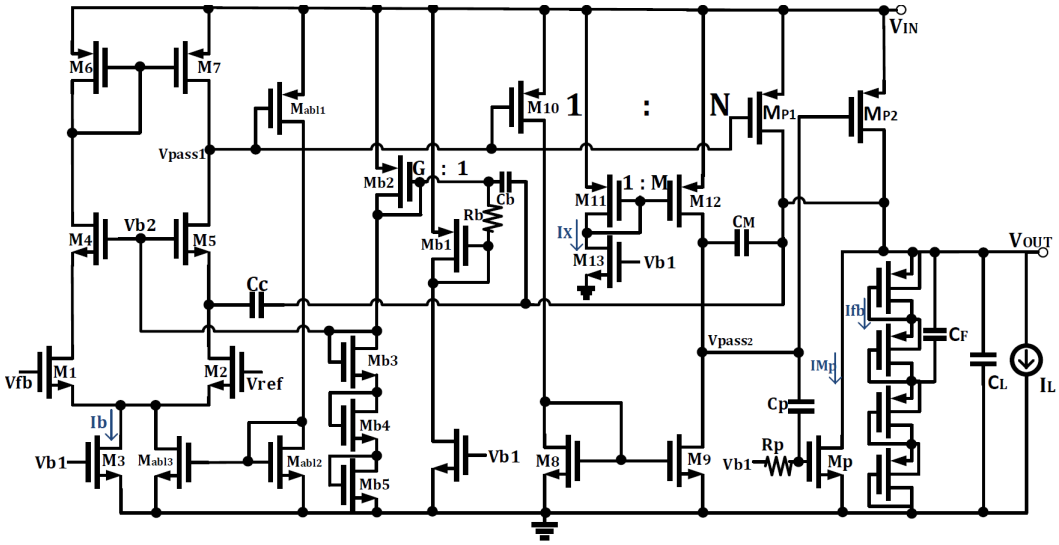


FIGURE 5.1: Schematic of the complete CL-LDO.

Design parameters	
C_C	$3pF$
C_M	$2pF$
Rb, Rp	$10M\Omega$
Cb, Cp	$2pF$
N	120
M	150
G	14
M_4, M_5	$6/0.06$
M_{abl3}	$1/0.06$
M_{P1}	$120/0.06$
M_{P2}	$2200/0.06$

TABLE 5.2: Key design parameters.

5.2 Simulation results

5.2.1 Quiescent current

Next table 5.3 summarizes the quiescent current that is consuming each block of the CL-LDO at no load condition.

Block	Quiescent current
Error amplifier	$450nA$
Gm boosting	$150nA$
Feedback network	$50nA$
Overshoot network	$100nA$
Second stage	$100nA$
Adaptive biasing loop	$50nA$
	900nA

TABLE 5.3: Quiescent current at no load current condition.

Fig. 5.2 shows the quiescent current through the entire range of load current (0 to 100mA). As it can be observed, during two stage operation, the quiescent current increases as a function of the load current, since the adaptive biasing loop senses the current of the pass device M_{P1}. When the LDO enters into three stage operation, the current through M_{P1} stops increasing and the main power transistor M_{P2} enters saturation region. Therefore, after this point, the quiescent current remains almost constant. Note that at maximum load current, the regulator achieves a current efficiency of 99.9%. The current efficiency is given by:

$$Current\ efficiency = \frac{I_{LOAD}}{I_{LOAD} + I_Q} \tag{5.1}$$

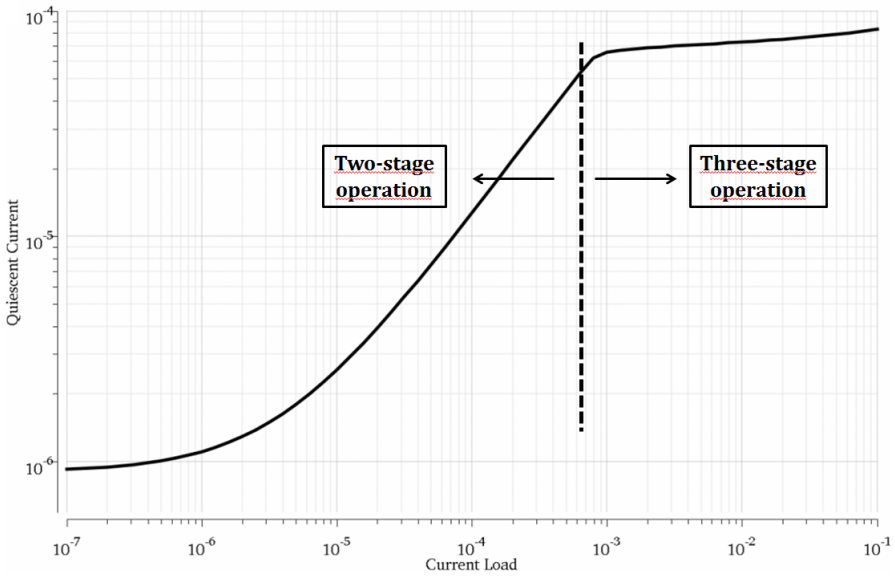


FIGURE 5.2: Quiescent current as a function of load current I_L. (30 points per decade).

5.2.2 Steady-state performance

As already commented in Chapter 2, there are two important parameters that define the steady-state LDO output regulation, the line and load regulations.

The load regulation determines the capability of the regulator to maintain the output voltage with steady-state variations in load current. Observe that when the regulator is operating as three stage, the output voltage approaches even more to the target voltage, since the open-loop gain is higher.

The line regulator determines the capability of the regulator to maintain the output voltage but with steady-state variations in input voltage. Fig. 5.4 represents the line regulator for both no-load and full-load condition of the capless LDO, 0 and 100mA, respectively. The calculated slope of no-load condition revels $4.6mV/V$ while the slope of full-load revels $1.3mV/V$.

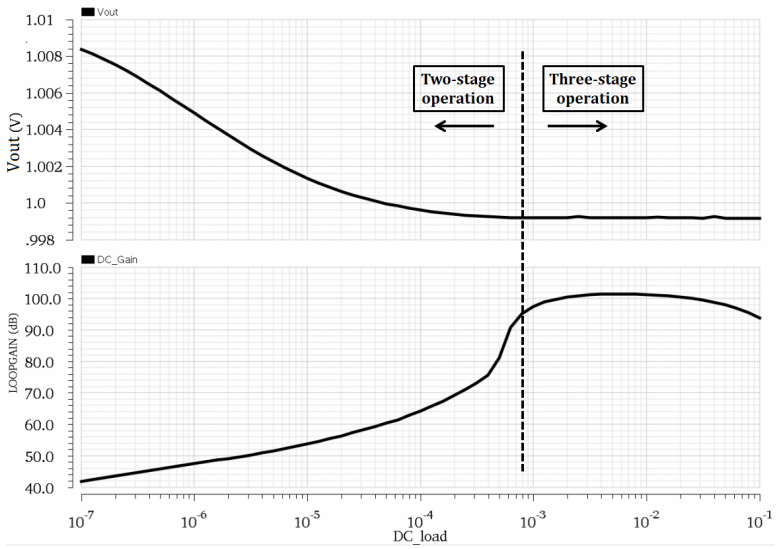


FIGURE 5.3: Load regulation response (top) DC gain (bottom) (30 points per decade).

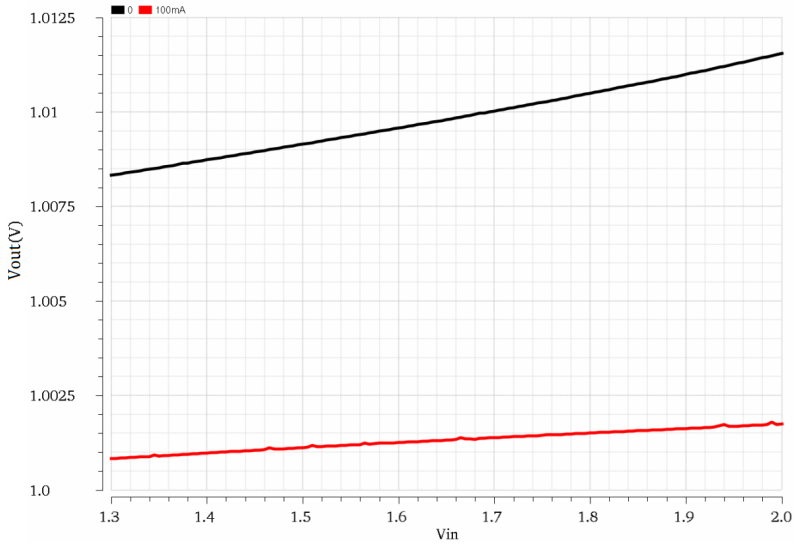


FIGURE 5.4: Line regulation respone (30 points per decade).

Conclusively, the line and the load regulation simulations show how small impact of the load current and the input variations have over the steady-state output voltage.

5.2.3 Dynamic-state performance

The transient response was simulated to evaluate both the line and load regulation in transient conditions. Fig. 5.5 illustrates the load transient response of the capless LDO. As expected, the output voltage suffers an overshoot to the $100mA \rightarrow 0$ load current transition, and undershoot to the $0 \rightarrow 100mA$ load current transition. The maximum overshoot and undershoot are $60mV$ (6%) and $-70mV$ (-7%), respectively. The settling-time

measured with approximately 0% of error is $5.6\mu s$ for the output voltage overshoot and $75ns$ for the output voltage undershoot case.

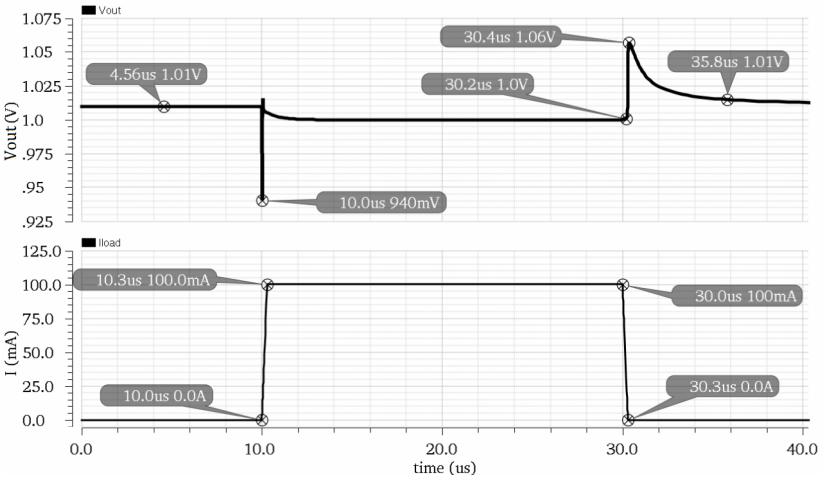


FIGURE 5.5: Load transient response.

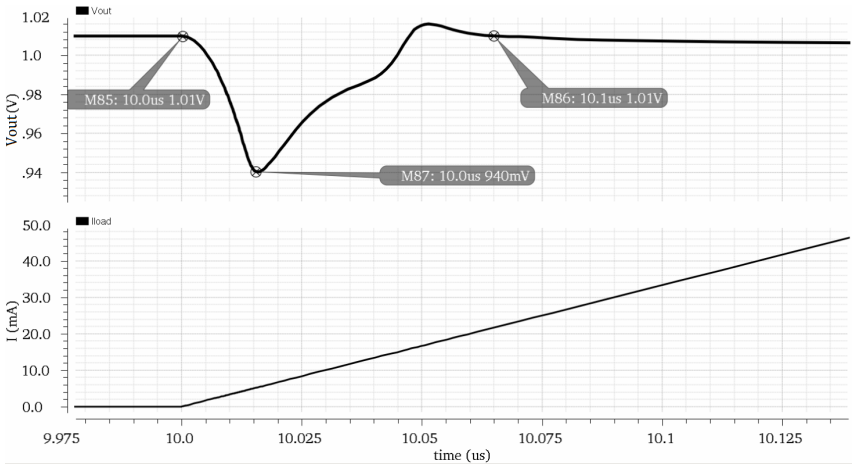


FIGURE 5.6: Zoomed-in view of the undershoot transition.

The line transient response is simulated in no-load condition (Fig. 5.7), changing the input voltage between $Vin = 1.3$ and $Vin = 1.5$ within $10\mu s$ edge time. The result shows a maximum positive and negative voltage spike of $25mV$ and $5mV$, respectively.

5.2.4 Stability

The loop gain and phase of the CL-LDO voltage regulator for different load current conditions are shown in Fig. 5.8. The output capacitance is fixed to the maximum value $500pF$ which is the worst-case scenario. At no-load condition, the regulator achieves a minimum loop gain of $40dB$. When the load current raises, the loop gain increases to approximately $100dB$. The phase and the gain margin are shown in Fig. 5.9. It shows that at no-load condition the phase margin and the gain margin are around $100°$ and $110dB$, respectively. However, as the load increases, the phase margin

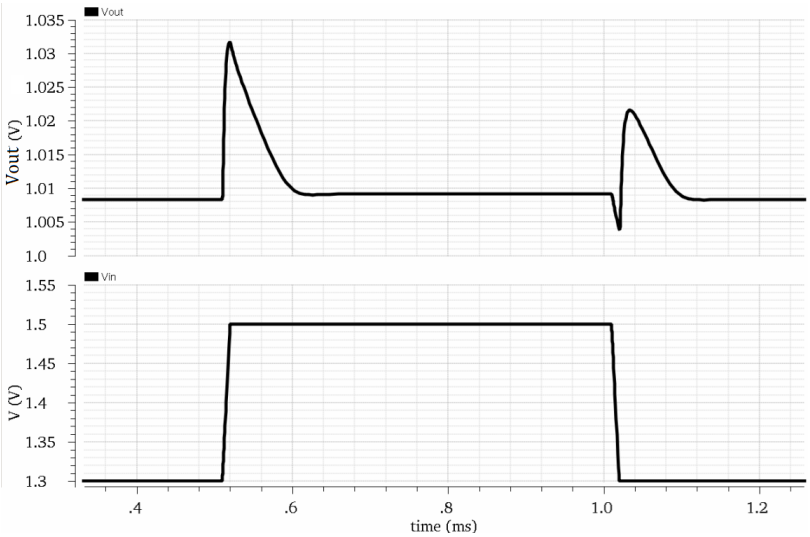


FIGURE 5.7: Line transient response.

decreases because of the gm-boost loop and the three-stage operation. Usually in LDO (two-stage) the worst-case scenario is given at minimum load current condition (as discussed in 2.3.2), because it is the point that both low-frequency poles (dominant and non-dominant) are closer together.

The gain-bandwidth (GBW) as a function of load current is shown in Fig. 5.10. The GBW is increased with the load current I_L due to the rise in the current bias of the error amplifier caused by the adaptive biasing loop which increases the transcondutance gm_1. See GBW equation repeated for convenience.

$$GBW = \frac{\beta gm_1}{C_C} \tag{5.2}$$

Conclusively, the CL-LDO stability is ensured for all load current conditions as the phase and gain margin are always greater than $55°$ and $28dB$, respectively.

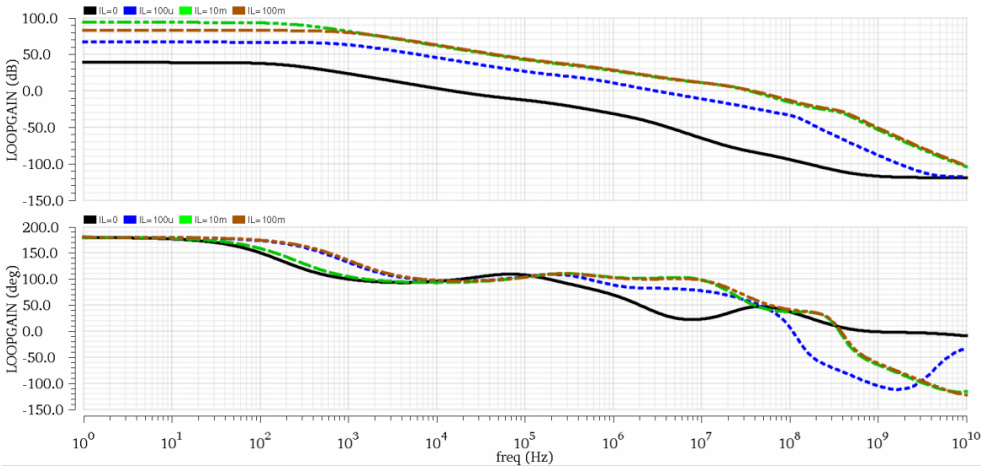


FIGURE 5.8: Frequency response over different load current I_L (30 points per decade).

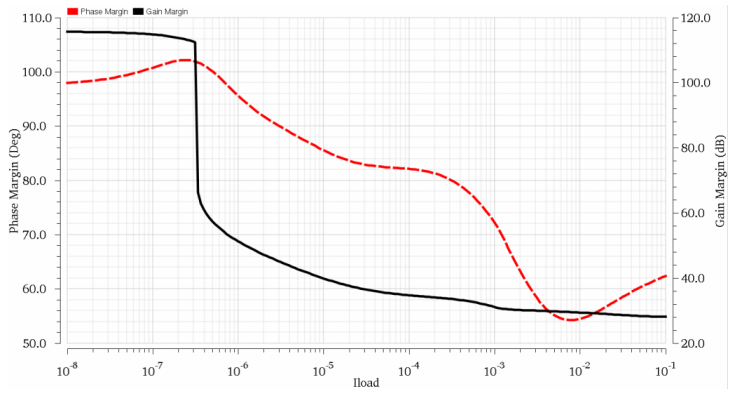


FIGURE 5.9: Phase and gain margin over different load current I_L (30 points per decade).

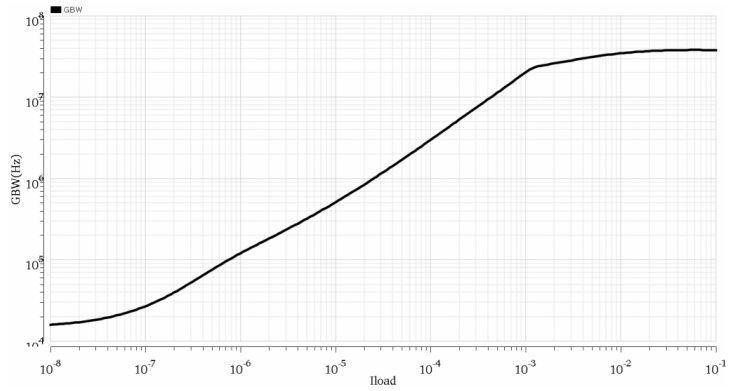


FIGURE 5.10: Gain-bandwidth over different load current I_L (30 points per decade).

5.2.5 Power supply rejection

The PSR for all load current condition from 0 to $100mA$ is presented in Fig. 5.11. At low frequencies, the difference between PSR curves is approximately $6dB$. At higher frequencies ($@10kHz$) and specially for light load current conditions, the PSR rapidly deteriorates. This is because the noise coming from supply is coupled through the source of transistor $Mb2$ and then amplified by the gm-boost loop gain.

In order to see how the gm-boost affects the PSR, a comparison is made with (Fig. 5.11) and without (Fig. 5.12) it. As it can be observed, during light load current conditions, i.e., when the regulator is in two stage operation, the PSR greatly differs between them. In two stage mode, the maximum value of PSR is -$5dB$ with the gm-boost and -$20dB$ without. On the other hand, when the regulator is in three stage mode, without the gm-boost it gives <-$40dB$ until $1MHz$; with gm-boost $-40dB$ are achieved around $100kHz$.

Fig.5.13a and 5.13b show the loop gain of the gm-boost loop (dashed-blue), the PSR with (black) and without (dotted-red) the gm-boost for light and high load current conditions, respectively. Note that whenever the gm-boost is used, the PSR will follow its loop gain.

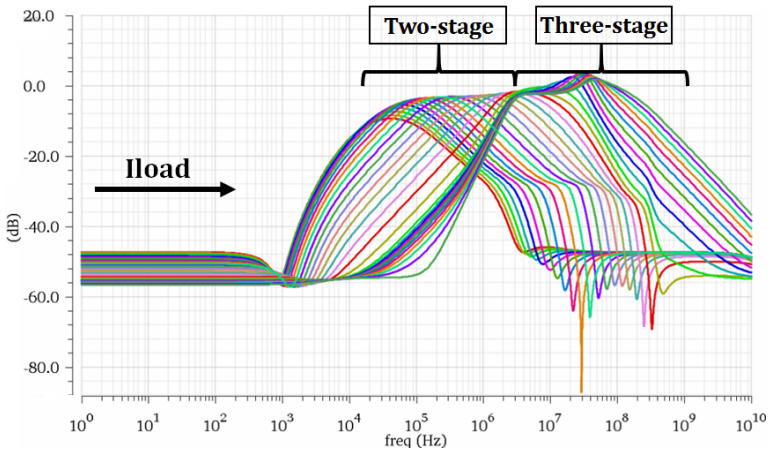


FIGURE 5.11: PSR with gm-boost.

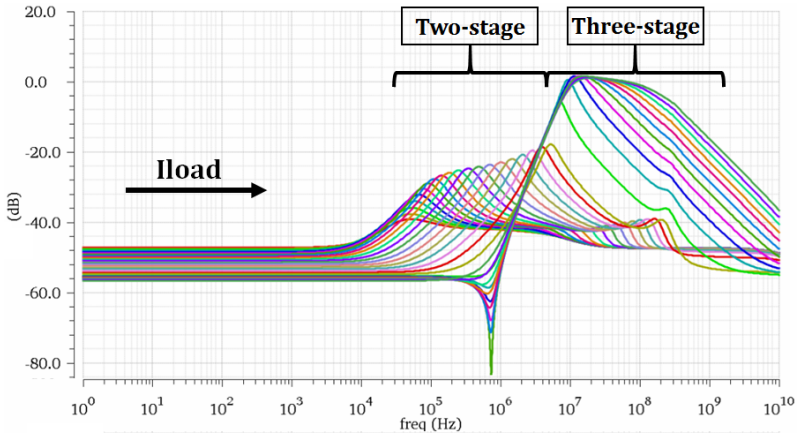
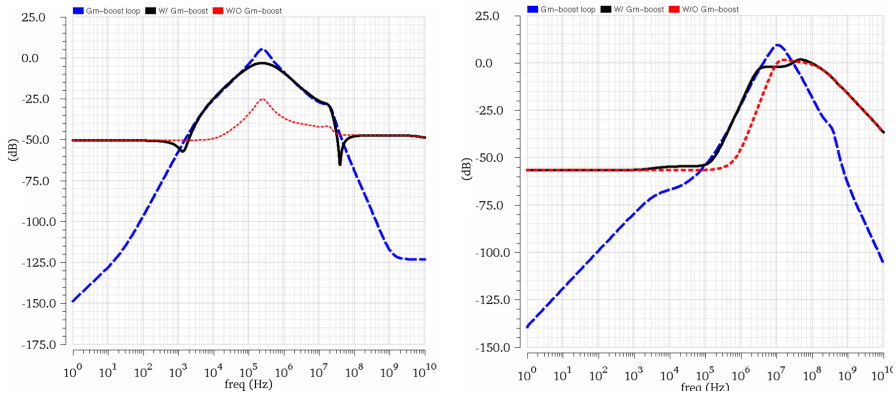


FIGURE 5.12: PSR without gm-boost.



(A) Low load current $10\mu A$ (B) High load current $100mA$

FIGURE 5.13: Gm-boost loop gain (blue), PSR W/ gm-boost (black), and PSR W/O gm-boost (red).

Fig.5.14 presents the PSR with the source of $Mb2$ isolated from Vin, as seen, the PSR is hardly affected by the gm-boost loop gain, since there is no other significant path in the gm-boost where the supply noise can couple.

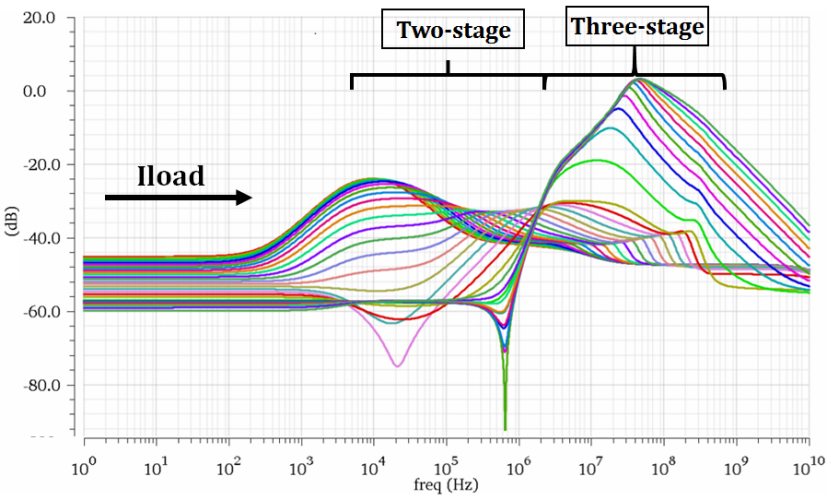
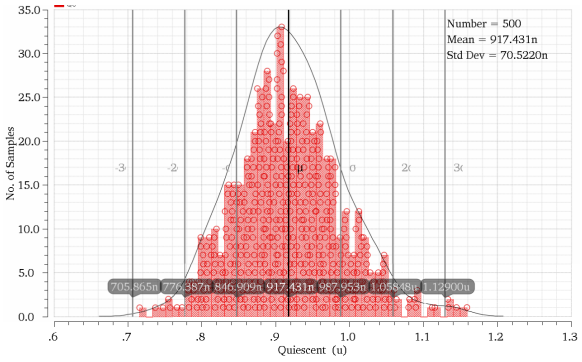


FIGURE 5.14: PSR with $Mb2$ source isolated from the input voltage.

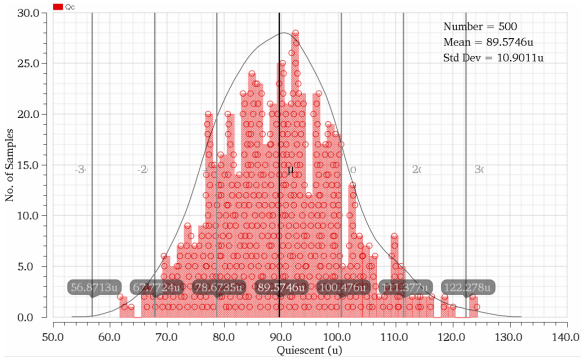
5.2.6 Monte Carlo analysis

Monte Carlo (MC) analysis is also performed in order to demonstrate the behavior of the CL-LDO under random fabrication process imperfections and mismatch effects.

Fig. 5.15 shows the Monte Carlo analysis of the quiescent current I_Q for both no-load and full-load conditions.



(A) no-load I_L



(B) full-load I_L

FIGURE 5.15: Quiescent current (500 samples).

As it can be observed, both parameters are quite sensitive to mismatch effects and process variations, especially at full-load current condition. These variations are mainly caused by the current comparator (second stage) and the adaptive biasing loop mismatch. Thus, the more activated the block (high current load), the higher the sensitivity of the quiescent current.

Fig. 5.16 illustrates the Monte Carlo analysis of the load transient response. A zoomed-in view of the undershoot transition is depicted in Fig. 5.17 for better visualization. In addition, Fig. 5.18 presents the overshoot and undershoot percentage of variation. As seen, their magnitudes are slightly aggravated. The worst-case overshoot/undershoot given in the analysis are 7.8% for both. However, as seen in Fig. 5.19, the DC output appears to be considerably more sensitive to mismatch effects. This is because of variations in the feedback network and specially in the input differential pair.

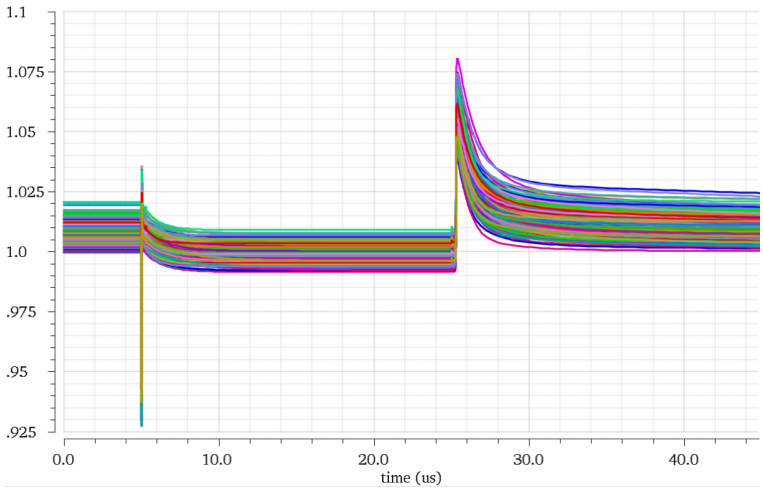


FIGURE 5.16: Load transient response (200 samples).

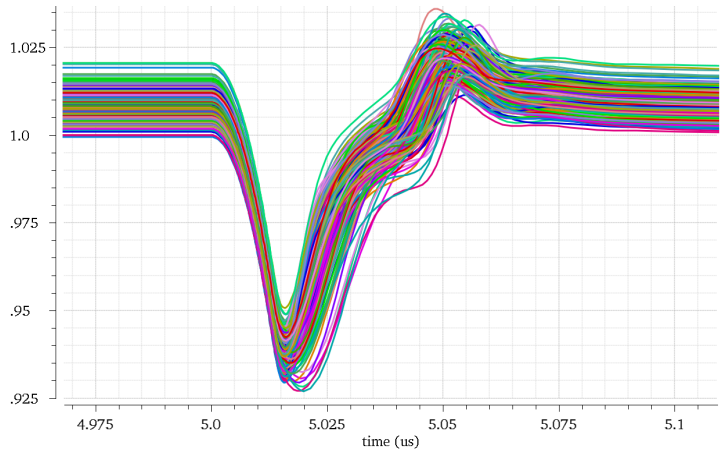
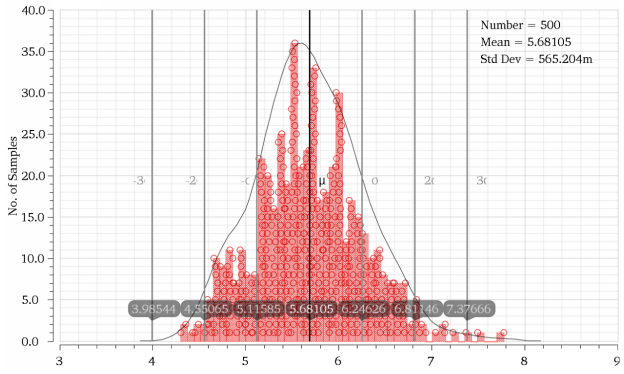
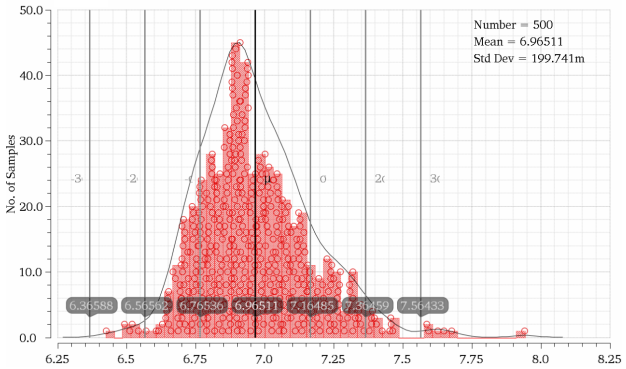


FIGURE 5.17: Zoomed-in view undershoot (200 samples).

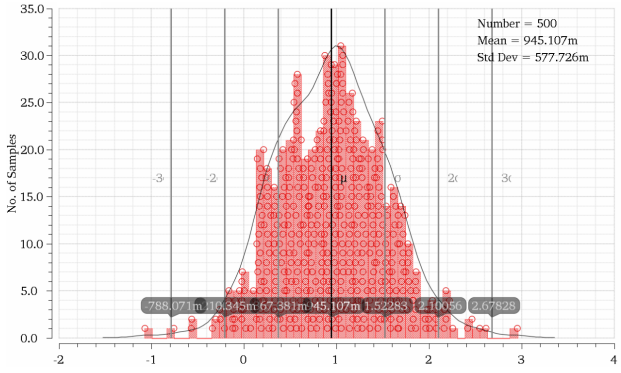


(A) Overshoot (%)

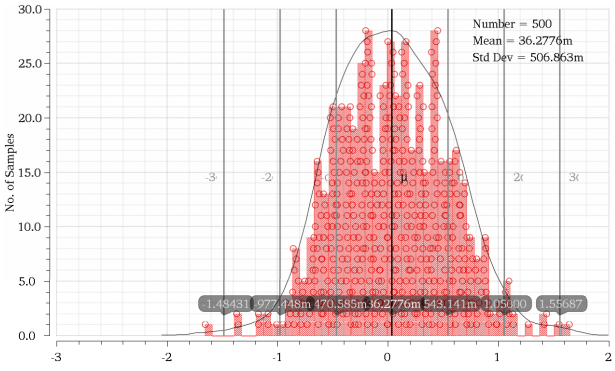


(B) Undershoot (%)

FIGURE 5.18: Undershoot/Overshoot (%) (500 samples).



(A) no-load I_L



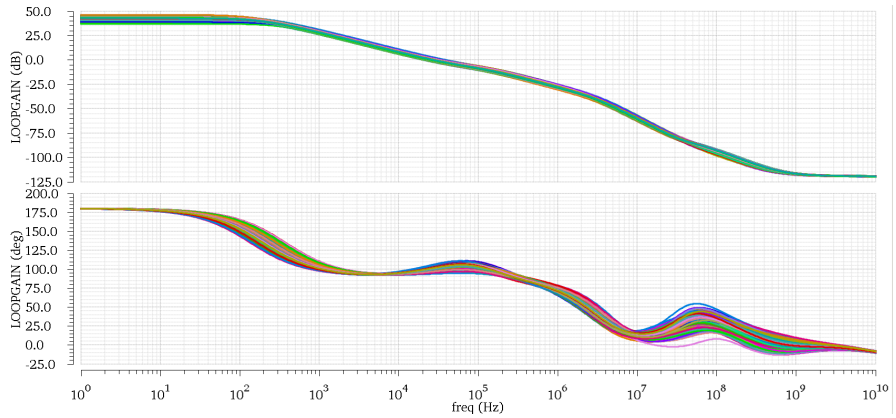
(B) full-load I_L

FIGURE 5.19: Output DC offset (%) (500 samples).

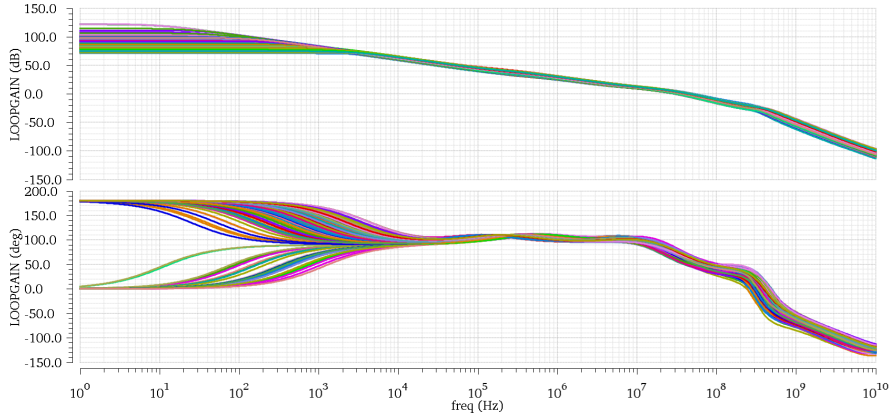
The Monte Carlo analysis of the frequency response for no-load (0) and full-load ($100mA$) current conditions are presented in Fig. 5.20. The gain and phase margin for both current load conditions are also given in Fig. 5.21 and 5.22, respectively.
As it can be seen, at full-load current condition the low frequency gain and the dominant pole are very sensitive to mismatch effects and process variations. This is due to variations in the bias current of the error amplifier that change the EA output resistance. As already commented above, these variations are mainly caused by the current comparator and the adaptive biasing loop mismatch, Consequently, the dominant pole (p_1) and the DC gain are variable in a range of $60°$-$120°$, and $20Hz$-$30kHz$, respectively

The phase DC value fluctuates between $0°$ and $180°$ at full-load case. It is due to the fact that there are other loops in the circuit that the stability analysis does not take into account such as the positive feedback. However, this is just an interpretation of the simulator and has no effect on the analysis and result.

Some samples of the phase margin for full-load condition fall below $60°$, which might be problematic. However, it remains above $45°$, which ensures the stability.

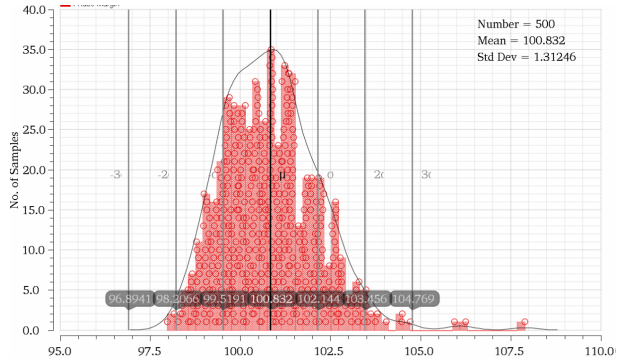


(A) no-load I_L

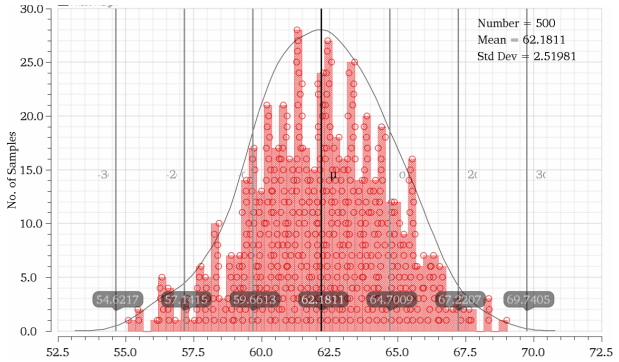


(B) full-load I_L

FIGURE 5.20: Frequency response over different load current I_L (200 samples).

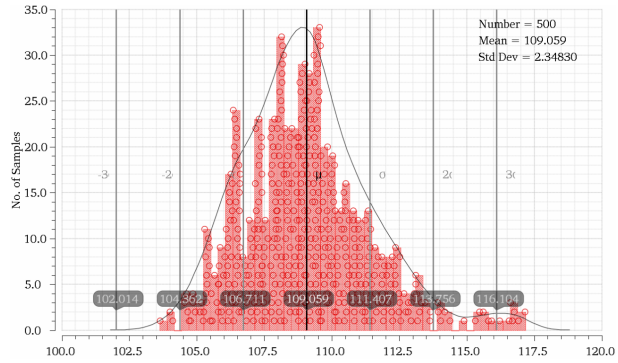


(A) no-load I_L

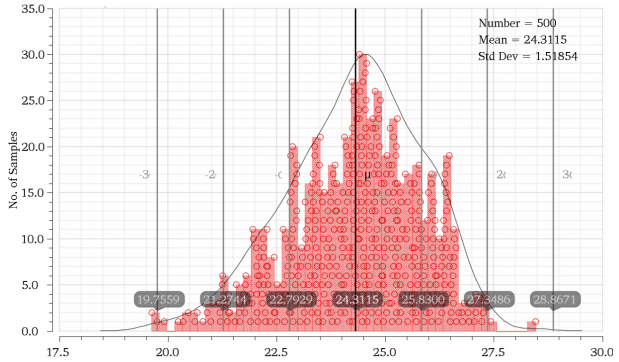


(B) full-load I_L

FIGURE 5.21: Phase margin (500 samples).



(A) no-load I_L



(B) full-load I_L

FIGURE 5.22: Gain margin (500 samples).

The Monte Carlo analysis of the PSR for no-load and full-load conditions are shown in Fig. 5.16 and 5.17, respectively. At no-load condition, the DC PSR presents a variation range around $8.5dB$ and all samples start to approach to each other as the frequency increases, except for the range $10kHz$-$10MHz$.

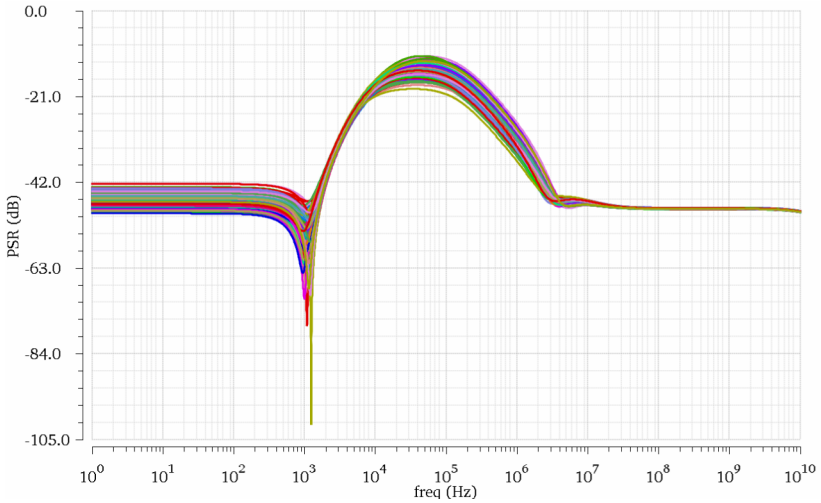


FIGURE 5.23: PSR no-load current condition.

At Full-load condition, the PSR is quite sensitive to mismatch effects and process variations. The DC PSR presents a variation range of $15dB$. However, all samples start to approach to each other as the frequency increases.

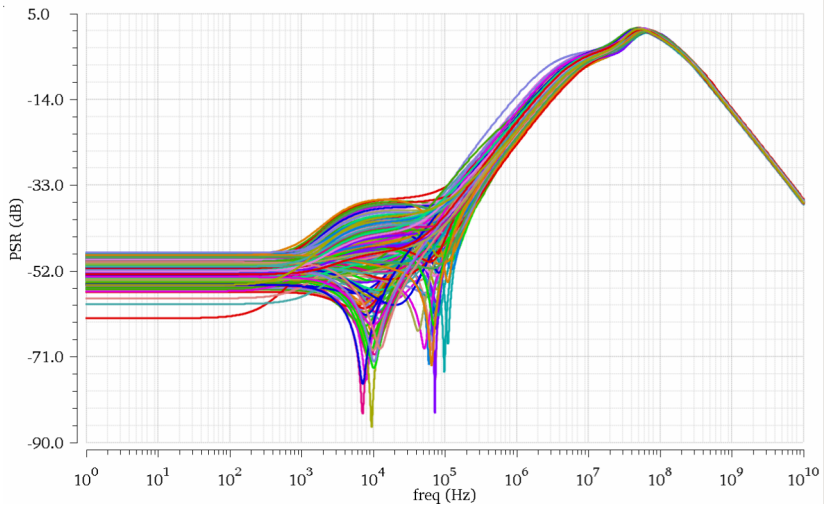


FIGURE 5.24: PSR full-load current condition.

5.2.7 Performance summary

The design specifications previosuly introduced at the beginning of this chapter, were all met. Table 5.4 summarizes and compares with the most relevant published works the overall performance based on the typical simulation results.

Parameters	This Work	[9]	[40]
$Year$	2016	2013	2015
$Technology$	$40nm$	$60nm$	$130nm$
$Pass\ device$	CS	CS	CS
$V_{IN}(V)$	1.4	1.2	1
$V_{OUT}(V)$	1	1	0.8
$V_{DO}(mV)$	400	200	200
$\Delta V_{OUT}(mV)$	70(7%)	68(7%)	120(15%)
$I_{L_{max}}(mA)$	100	100	100
$I_{L_{min}}(\mu A)$	0	0	1
$I_{Quiescent}(\mu A)$	0.9	0.9	2.9
$C_{OUT}(pF)$	500	100	100
$t_{rise}(ns)$	300	300	800
$t_{settle}(\mu s)$	5.6	5	1.7
$PM_{min}(°)$	55	-	-
$GM_{min}(dB)$	28	-	-
$FOM_1(ps)$	0.003	0.0006	0.0035
$FOM_2(mV)$	0.0006	0.0006	0.0017

TABLE 5.4: Performance comparison of the proposed CL-LDO with most relevant published works.

5.2.8 Extreme case Load transient regulation

Usually, the main purpose for an LDO is the ability to supply low-voltage digital circuitry.

For simulation purpose a load of $20k$ logic gates (AND) switching simultaneously with a $5MHz$ clock was modeled. Table 5.5 compares the current pulse characteristics of this digital model to the one given in table 5.1 at the beginning of this Chapter.

Parameter	Digital Model	Proposed 5.1
Max current spike	$23mA$	$23mA(100mA)$
$t_{rise/fall_{min}}$	$550ps$	$69ns(300ns)$
Pulse width	$90ns$	$20\mu s$

TABLE 5.5: Comparison between digital model and proposed pulse currents.

Evidently, the load current characteristics of this model will produce worse response in the CL-LDO. Compared to the characteristics given in table 5.1, the rise/fall time $t_{rise/fall}$ is 125 times faster and the pulse width is 220 times reduced.

Even given these circumstances, the output voltage only fluctuates between $1.12V$ and $930mV$, as shown in next Fig. 5.25.

When the current load suddenly decreases and remains to 0, the output voltage needs long time to recover to the target voltage ($1V$), since the current injected by the overshoot reduction network is much less due to slewing effects at the gate of the pass device M_{P2} (V_{pass2}).

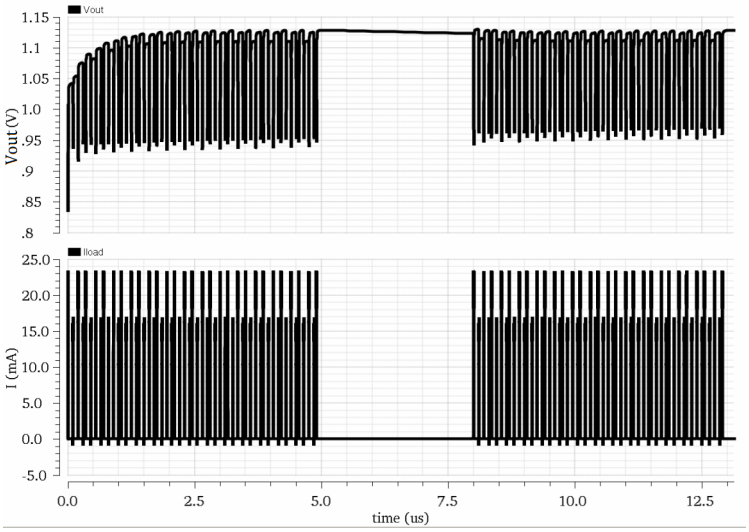


FIGURE 5.25: Load transient response with digital model: V_{out} (top) and current pulses (bottom).

A zoomed-in view of the first two current pulses is illustrated in Fig. 5.26 below.

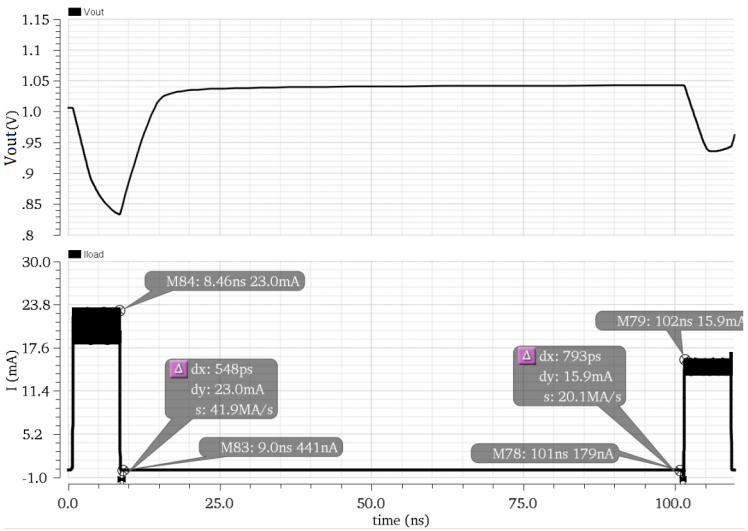


FIGURE 5.26: Load transient response zoomed-in view of the first two current pulses.

Chapter 6

Conclusions

6.1 Summary and conclusions

In this thesis work the design and limitations of capacitor-less LDO regulators were analyzed. A regulator has to be able to regulate the output voltage under fast variations in the load current as well as in the input supply with extremely low power consumption. The specifications were defined based on the State-Of-The-Art research. Several published techniques were carefully analyzed, simulated and used in order to achieve a CL-LDO that meet the targeted performance.

The small-signal behavior of the regulator for both modes of operation (two-stage and three-stage) has been accurately analyzed as well as verified by both simulation and calculation. Based on the three-stage small signal model, a Nested-Miller compensation which can reduce the Q-factor significantly is proposed. Furthermore, the large-signal analysis to fast load current transitions is also given for both the undershoot and overshoot where a Gm-Boost circuitry is proposed to improve the undershoot.

The CL-LDO was designed in TSCM $40nm$ Low Power (LP) CMOS technology. The simulated results shows that the regulator achieves the given specifications. With this performance, the proposed CL-LDO regulator could provide a viable solution for low-voltage, low power consumption, SoC applications, while reducing overall cost.

6.2 Future work

Due to the time limit and the different possible combinations of trade-offs, several aspects of this work have not been fully improved. The main relevant are mention in the following.

- *PSR response* $\Rightarrow$ The Gm-Boost highly affects the PSR response at medium/high-frequencies.
- *P-V-T simulation* $\Rightarrow$ The final design behavior must be validate over process corners, temperature and supply variations.
- *Adaptive biasing loop and current comparator* $\Rightarrow$ They are very sensitive to process parameters variations and mismatch. They may further improved by increasing the dimension of the transistors (rises a problem of dynamic performance).

  Additionally, current replica mirror [29] can be added to ensure that pass device M_{P1} and the mirror transistors M_{abl1}, and M_{10} are in the

same region of operation (Vgs and Vds for both devices are equal). However, it requires more area and current consumption.

- *Output offset* ⇒ The DC output is quite sensitive to mismatch effects due to variations in the feedback network and specially in the input transistors M_1 and M_2.

- *Over-voltage protection* ⇒ An increased in the input voltage is a serious issue of the breakdown limits of the transistors, especially for the thin-gate-oxide which have lower breakdown voltage. To solve this problem, controlled cascode thick-gate-oxide transistors can be added in series to reduce the voltage drop [36]. The disadvantages are that it requires additional circuitry to control the cascodes as well as the performance of the regulator may be affected. Other solution exists such as, using a switching regulator to supply the LDO, this would bring down the power supply so reducing the operating voltage of the LDO. However, this would lead to area and cost increased.

- *Gm-Boost loop response time* ⇒ The bandwidth of the gm-boost is very sensitive to parasitics, specially at V_{b2}.

- *Nested-Miller compensation* ⇒ The proposed capacitor C_M causes slewing effects at the gate of the pass device M_{P2} which degrade the overshoot and the settling-time. Cascode compensation can be used instead, by adding cascode transistors into the second stage (current amplifier). Therefore, as already explained in section 4.2, the capacitor is isolated from the output node to the gate of the pass device $Vpass2$.

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